Journées scientifiques du PEPR Électronique

17-21 mars 2025

Cité des sciences et de l'industrie - Paris

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ADICT
PAC
CHOOSE

PRÉSENTATION DU PEPR

CONTEXTE

L'électronique est au cœur des fonctionnalités numériques des produits et services dans nos sociétés et devient un enjeu stratégique, faisant l'objet de forts risques de prise de contrôle que ce soit par des industriels étrangers ou d'autres états.

C'est fort de ce constat que le gouvernement a fait de l'électronique un choix prioritaire dans sa stratégie nationale de recherche et de développement technologique et industriel. Il a notamment confié au CNRS et au CEA le pilotage du PEPR (Programmes et Equipements Prioritaires de Recherche) Électronique visant à générer des innovations pour accélérer la croissance et relocaliser certaines productions en France ou en Europe grâce à des solutions technologiques nouvelles et ce, de manière durable sur le plan économique comme sur le plan écologique.

OBJECTIFS

Créer et soutenir des filières technologiques nationales, dans les laboratoires académiques à fort potentiel industriel
Stimuler le développement de technologies à un niveau de maturité convaincant (TRL 4)
Regrouper des compétences scientifiques dispersées au niveau national
Impulser une convergence matériau-compo-sant-sous-système entre des équipes de recherche pertinentes

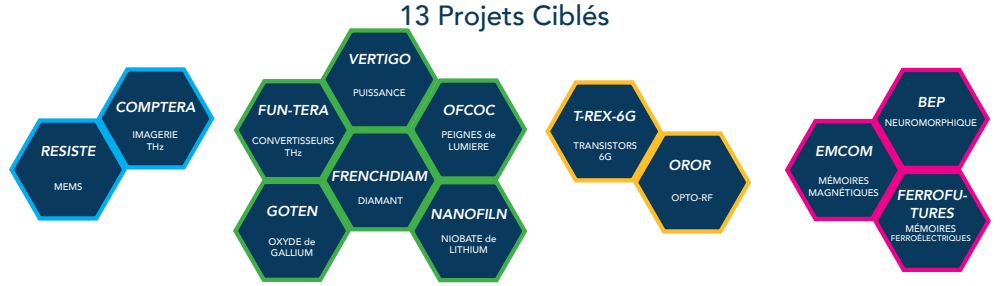
2 VOLETS

1 VOLET DE RENFORCEMENT et mise à niveau des équipements de micro-nanofabrication du réseau RENATECH piloté par le CNRS et de la plateforme de nano-caractérisation PFNC du CEA dans les laboratoires académiques, et 1 VOLET SCIENTIFIQUE autour des 4 grandes thématiques. 9 projets ciblés et 3 actions transverses ont démarré en septembre 2022. 4 nouveaux projets (suite à l'appel ouvert en Juin 2023) complètent ce volet depuis avril 2024.

VUE D'ENSEMBLE

4 thématiques, 13 projets, 3 actions transverses, 2 projets d'investissement

13 Projets Ciblés



3 Actions Transverses

2 Projets d'Investissement

LES DIRECTEURS DE PROGRAMME ET LES COPILOTES DU PEPR

Isabelle SAGNES
CNRS

Thomas ERNST
CEA

	CNRS/Universités	CEA
RESISTE	Nicolas TIERCELIN	Sophie GIROUD
COMPTERA	Carlo SIRTORI	Laurent DUSSOPT
VERTIGO	Cyril BUTTAY	Julien BUCKLEY
GOTEN	Ekaterine CHIKOIDZE	Eva MONROY
FRENCHDIAM	David EON Karine ISOIRD	Cédric MASANTE
OFCOC	Christian GRILLET Yoan LÉGER	Vincent REBOUD Quentin WILMART
NANOFILN	Mathieu CHAUVET Olivier GAUTHIER-LAFAYE	Soazig LEFORESTIER
FUNTERA	Guillaume DUCOURNAU	Éric MERCIER
T-REX-6G	Mohammed ZAKNOUNE	Thierry BARON Hervé BOUTRY
ORÒR	Mehdi ALOUINI	Leopold VIROT
EMCOM	Manuel BIBES	Kevin GARELLO Louis HUTIN
FERROFUTURES	Cristell MANEUX	Jean-Philippe NOEL
BEP	Daniel BRUNNER Damien QUERLIOZ	Élisa VIANELLO
ADICT	Philippe BOUCAUD	Matthieu JAMET
CHOOSE	Ian OCONNOR Pascal VIVET	Lorenzo CIAMPOLINI
PAC	Thomas BARON Hugues GRANIER	David HENRY

PROGRAMME DU MARDI 18 MARS

08h00 – 08h30	Accueil badges
08h30 – 09h00	Accueil café
09h00 – 09h45	Introduction de la journée : **Amandine Reix** - DGE - **Hervé Martin** - MESR, **Sebastien Dauvé** - CEA-Leti, **Lionel Buchaillot** - CNRS Ingénierie, **Jean-Philippe Bourgoin** - Agence ASIC-CEA
09h45 – 10h15	Synthèse des activités du PEPR : **Isabelle Sagnes** - CNRS, **Thomas Ernst** - CEA
10H15 – 10H45	L'électronique pour le numérique : RESISTE & COMPTERA
10h45 – 11h15	Pause
11h15 – 12h30	L'électronique pour les télécommunications : T-REX-6G, ORÒR L'électronique pour la convertion : FUN-TERA Action transverse : PAC
12h30 – 13h30	Déjeuner
13h30 – 15h15	Ouverture congrès C'Nano / Session du jeu «La fabrique du Nano»
15h15 – 15h45	Keynote speaker : **Lisa Michez** - Aix Marseille Université "Les altermagnets, une nouvelle opportunité pour la spintronique"
15h45 – 16h00	Présentation du PEPR SPIN : **Vincent Cros** - CNRS, **Lucian Prejbeanu** - CEA
16h00 – 16h30	L'électronique pour le calcul : EMCOM Action transverse : ADICT
16h30 – 17h00	Pause
17h00 – 18h30	L'électronique pour le calcul : BEP, CHOOSE, FERROFUTURES L'électronique pour la convertion : VERTIGO, GOTEN, FRENCHDIAM
19h30 – 21h00	Cocktail dinatoire musical

PROGRAMME DE LA SEMAINE

PROGRAMME ET PLANNING JOURNEES SCIENTIFQUES ET CONGRES C'NANO - 17/21 mars 2025

		Amphi Louis Armand 1 (Est)	Grand Amphi	Espaces canapés -3	Salle Commissariat général blanche	Salle Commissariat général rouge	Salle 1	Salle 2	Salle 3	Salle 4
Lundi 17 mars	après-midi				EQUIPEX NANOFUTUR					
Mardi 18 mars	8:30 - 9:00	Accueil des participants								
	9:00 - 9:45	Introduction de la journée Amandine Rex (DGE), Hervé Nifenecker (MESR), Sébastien Dauvé (CEA-Leti), Lionel Buchaillot (CNRS Ingénierie), Jean-Philippe Bourgoin (Agence ASIC-CEA)			Réunion CHOOSE					
	9:45 - 10:15	Synthèse des activités du PEPR : Isabelle Sagnes - CNRS & Thomas Ernst - CEA								
	10:15 - 10:45	Électronique pour le numérique : RESISTE & COMPTERA								
	10:45 - 11:15	Coffee break								
	11:15 - 12:30	L'électronique pour les télécommunications : T-REX-6G, OROR L'électronique pour la conversion : FUN-TERA Action transverse : PAC			Réunion CHOOSE					
	12:30 - 13:30	Lunch								
	13:30 - 14:00		Ouverture du Chaos Comme Chanson et Sébastien Bidault	Jeu la Fabrique du Nano					NANOCARAC Analyse structurale et morphologique	
	14:00 - 15:00		Intervention Pr. Emiliano CORTÉS, Univ of Munich, Nanoinstitute Munich					NANOCARAC Analyse 3D et traitements numériques		
	15:15 - 15:45	Keynote speaker Lisa Michez, Aix Marseille Université					NANOCARAC Analyses par méthodes optiques			
	15:45 - 16:00	Intervention PEPR SPIN : Vincent Cros (CNRS) Lucian Prejbeanu (CEA)								
	16:00 - 16:30	L'électronique pour le calcul : EMCOM Action transverse : ADICT								
	16:30 - 17:00	Coffee break								
	17:00 - 18:30	L'électronique pour le calcul : BEP, CHOOSE, FERROFUTURES L'électronique pour la conversion : VERTIGO, GOTEN, FRENCHDIAM)								
	19:30 - 21:00	Dîner Musical								
Mercredi 19 mars	matin			Jeu la Fabrique du Nano					Workshop de Nanocaractérisation	
	après-midi	Lunch						Réunion NANOFILN		Réunion GOTEN
		Session nanophotonics et nanoptics L'électronique pour la conversion : OFCOC, NANOFILN						Réunion FERROFUTURES	Réunion PAC inter-projets PEPR	NANOFILN industriels
Jeudi 20 mars	9:00 - 10:30	Présentation flash posters		Jeu la Fabrique du Nano				Réunion OFCOC		Réunion OFCOC
	10:30 - 11:00	Coffee break								
	11:00 - 12:30	Présentation flash posters		Jeu la Fabrique du Nano			Réunion EMCOM ET BEP			Réunion VERTIGO
	12:30 - 13:30	Lunch								
	après-midi					Réunion ADICT	Réunion PAC			Réunion ORORT
	19:00 - 23:30	Dîner de Gala Musical			Réunion FUN-TERA			Réunion RESISTE		Réunion FUN-TERA
Vendredi 21 mars	matin	Cérémonie de prix des 8 meilleurs posters			Dîner de Gala Musical			Lunch		Gala Musical
					Lunch					Lunch

PEPR électronique
Réunions consortium
Réunions industriels
Nanocaractérisation
Session commune
Session jeu La fabrique du Nano

LES LAURÉATS DES PRIX DES POSTERS

Aurélie FOURNIER
du LPENS pour COMPTERA

4

Adrien BIDAUD
de l'IEMN pour VERTIGO

11

Yannis BILLIET
de l'INL pour OFCOC

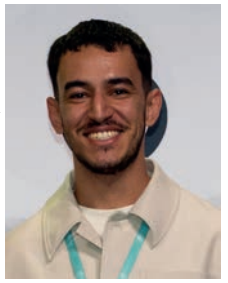
15

Nelly SCHEIBEL
de FEMTO-ST pour NANOFILN

27

Mohamed NADRANI
de l'IES pour ORORT

37

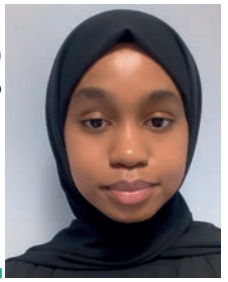


Hiba LAHLIMI-ALAMI
de XLIM
pour PAC / FUNTERA

62

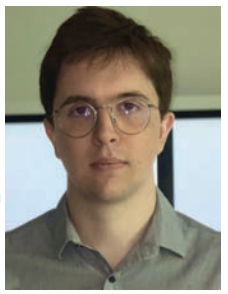
Mamadou Hawa DIALLO
de l'IM2NP pour BEP

51



Lucas MARTIN WISNIEWSKI
de l'IM2NP pour
FERROFUTURES

57



LA PERCEPTION NUMÉRIQUE

Projet RESISTE

IEMN | LAAS | IMS | IES | CEA-Leti | ESYCOM | CRHEA | GREMAN

Le projet RESISTE vise à développer une filière nationale spécifique aux capteurs micro-électromécaniques MEMS destinés à fonctionner en environnement sévère où règnent par exemple de hautes températures, des atmosphères corrosives, des radiations, des forces ou des accélérations très élevées. Dans ces situations, les capteurs MEMS traditionnels à base de silicium ne sont plus adaptés, ce qui nécessite une nouvelle approche. Des matériaux, comme le diamant et le carbure de silicium en couche mince ou substrat, ont des propriétés critiques liées aux contraintes des environnement sévères qui surpassent celles du silicium. Ils sont au cœur du projet RESISTE qui relèvera les défis rencontrés dans le développement des nouvelles filières technologiques associées à trois domaines d'application : l'anémométrie d'écoulements extrêmes, la mesure d'hyper-accélérations et la détection de composés chimiques en milieu radioactif.

Projet COMPTERA

IEMN | LPENS | IMS | CEA-Leti | LC2

L'imagerie THz connaît un essor important en lien avec le développement des technologies de composants intégrés semi-conducteurs et photoniques. Les applications sont nombreuses et touchent à des domaines stratégiques pour l'industrie nationale.
COMPTERA vise le développement de composants avancés pour les futurs systèmes d'imagerie multispectrale en gamme THz (0,3-30 THz) qui feront appel à des technologies très variées à la frontière de l'électronique et de l'optoélectronique, en particulier des détecteurs à haute sensibilité adaptés à chaque gamme de longueurs d'onde (notamment micro-bolomètres, détecteurs à effet de champ, photodétecteurs unipolaires à multi-puits quantiques). Une partie de ces capteurs ultra-sensibles sera ensuite intégrée à des systèmes d'imagerie adaptés à la démonstration de leurs performances.

RESISTE

Quentin David[1,2], K. Azaiez[2], F. Barcella[1], S. Chenot[2], I. Dufour[3], F. Mathieu[4], J-F. Michaud[1], D. Alquier[1], M. Portail[2]

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1

Towards SiC-based CMUT transducers for detection in harsh environments

Capacitive Micromachined Ultrasonic Transducers (CMUTs) are Micro-Electro-Mechanical Systems (MEMS) that can be used to generate and sense acoustic signals. An elementary CMUT cell functions as a variable capacitor. It consists of a suspended membrane above a cavity maintained under vacuum, located between a top electrode and the substrate. CMUTs are used in a variety of fields, including medical applications (therapy and imaging), physical sensors and gas detectors[1]. For the latter application, CMUT technology offers several advantages, including absence of sensing layer, high selectivity, sensitivity and resolution[2]. However, CMUTs are classically elaborated using silicon (Si) or dielectric material which are not suitable for a use under harsh environment conditions (temperature, radiation…).

As silicon carbide (SiC) is a robust material, offering greater resistance under extreme conditions, the use of SiC on Si substrates can be the basis to elaborate 3C-SiC-based cMUTs that could be helpful to circumvent the issues encountered with silicon[3]. However, to date, no CMUT based on high quality SiC material has been presented in the literature[4]. In this context, this work aims to design and fabricate an advanced SiC-based CMUTs, by different approaches, based on epitaxy, surface micromachining and/or wafer bonding techniques[5].

We will present our approaches and the current experimental developments conducted for handling CMUTs first fabrication steps.

On one hand, growth by Chemical Vapor Deposition (CVD) of specific Si/SiC/Si heterostructures and its temperature dependence will be introduced. We will then focus on the structural and morphological evolution with growth temperature. On the other hand, the bonding approaches will be discussed and we will show preliminary steps of SiO_2 deposited by Plasma-Enhanced CVD (PECVD) on 3C-SiC/Si templates.

References:
1. J. Joseph et al., IEEE Trans. Ultrason. Ferroelectr. Freq. Control (2021) 69, 456-467
2. L. Iglesias et al., Sci. Rep. (2022), 12:744
3. G. Ferro, Crit. Rev. in Sol. State and Rel. Mat. (2015) 40, 56-76
4. J-F. Michaud et al., Mater. Sci. Semicond. Process (2024) 171, 107986
5. M. Portail et al., Mater. Sci. Forum (2022) 1062, 94-98

Acknowledgement: Thanks to the RESIST project, financially supported by the French National Research Agency (ANR), under grant agreement No. ANR-22-PEEL-0002 and Nanofutur

RESISTE

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3. ESYCOM, CNRS, Univ Gustave Eiffel, Marne-la-Vallée, France

2

Diamond membrane resonators

Diamond growth technology offer a way to produce MEMS structures. Here we present a fabrication technology and characterization of a diamond membrane-based sensor. Circular membrane with diameter of 850 µm and thickness of intrinsic diamond in the range of 3566 nm to 4964 nm were successfully fabricated with integrated piezo resistive gauges for embedded electrical measurement. Resonance frequencies both in air and liquid phases were measured with a Laser-Doppler profilometer using piezo excitation. Calculation and simulation results aligned closely with experimental results of membrane resonance frequency. Values of resonance frequency in the air and in DI were measured to be 153.5 kHz - 254.0 kHz and 34.4 kHz – 65.3 kHz, respectively. We also report our study on boron-doped diamond (BDD) mechanical transducer. An overall assessment of size and thickness versus performance is presented. The optimum BDD membranes were selected based on their minimal noise in liquid medium. These membranes are measuring 1000 µm in diameter and featuring a thickness of 2.6 to 3.2 µm. This work illustrates the promising potential of diamond-based sensors. This technology could be extended in various fields such as harsh environment, healthcare diagnosis and volatile compound detection.

References:
- Zhang, M. et al. Synchronization of Micromechanical Oscillators Using Light. Phys. Rev. Lett. 109, 233906 (2012).
- Zhang, M., Shah, S., Cardenas, J. & Lipson, M. Synchronization and Phase Noise Reduction in Micromechanical Oscillator Arrays Coupled through Light. Phys. Rev. Lett. 115, 163902 (2015)
- Colombano, M. F. et al. Synchronization of Optomechanical Nanobeams by Mechanical Interaction. Phys. Rev. Lett. 123, 017402 (2019).

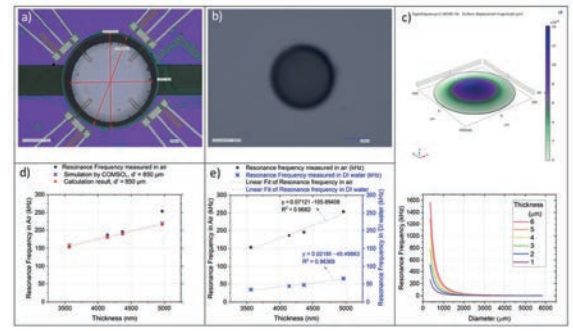

Figure 1 a) Microscope image of fabricated intrinsic diamond membrane with piezo resistivity gauges integrated b) Microscope image of fabricated BDD membrane c) Simulation result of the fundamental mode of a circular membrane with fixed edge d) Correlation between thickness of intrinsic diamond membranes and resonance frequency in air and DI water e) Comparison between experiment, calculation and simulation results.

Acknowledgement: ANR-22-PEEL-0002 and Nanofutur

RESISTE

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3 Impact de la dimension de la cavité et des fils sur les paramètres de l'accéléromètre thermiqueors

Depuis de nombreuses années, de nombreux types d'accéléromètres ont été développés pour mesurer des vibrations et des chocs. Ces capteurs sont largement utilisés dans le domaine de l'aviation, ainsi que dans l'industrie automobile, comme pour la détection des collisions par les airbags ou dans des applications de défense [1].
Les accéléromètres thermiques sont composés d'un fil chaud positionné au centre d'une cavité remplie de gaz. De chaque côté du fil chaud, se trouve deux fils de détection (Figure 1a). Cette architecture permet de mesurer des grandes accélérations (jusqu'à 10 000g). Sous l'influence d'une accélération Γ, le profil de température est modifié, et le gradient thermique, initialement symétrique de part et d'autre du fil chaud, se voit déformé. Cela à pour effet de créer une différence de température entre les détecteurs δT, proportionnel à l'accélération subit (Figure 1b). La sensibilité du capteur S, est donnée par $S = \delta T/\Gamma$ (°C/g) [1].
Une étude de la sensibilité a été menée par simulation CFD (Figure 1c), d'abord sur des modèles 2D simples, puis sur des modèles réels en 3D. l'objectif à été de déterminer l'évolution de la sensibilité des capteurs en fonction de l'accélération subit, pour plusieurs dimensions de la cavité. Les résultats ont permis d'obtenir la plage de mesure des capteurs, dans la zone linéaire du graphique LogLog (Figure 2) [2].
La bande passante des capteurs a aussi été étudiée, de façon numérique et expérimental. Cela a permis de mettre en évidence l'impacte de la présence des fils de détection, par rapport à une cavité seule, sur le temps de réponse des accéléromètres (Figure 3). L'étude a été réalisée pour plusieurs couples taille de détecteurs/taille de cavité. Le temps de réponse des fils seul a aussi été étudié expérimentalement.

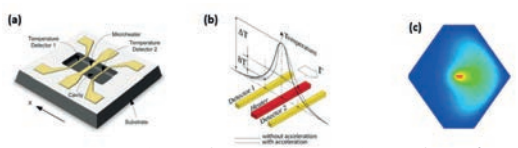

Fig.1 : (a) Structure d'un accéléromètre thermique basé sur le transfert thermique convectif. (b) Profil de température avec et sans accélération. (c) Simulation CFD du profil de température sous l'influence d'une accélération.

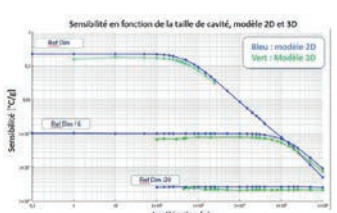

Fig.2 : (a) Comparaison entre le modèle 2D et 3D des résultats de simulation CFD sur l'évolution de la sensibilité en fonction de l'accélération, pour plusieurs tailles de cavité.

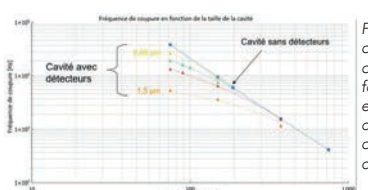

Fig.3 : (a) Impacte de la présence des détecteurs en fonction de leur taille et de la taille de la cavité, sur le temps de réponse des capteurs.

References:
[1] A. Garraud, « Amélioration des performances et nouveau concept de détecteurs de capteursinertiels à détection thermique », Université Montpellier II - Sciences et Techniques du Languedoc,Montpellier, 2011.
[2] A. Garraud, P. Combette, J. M. Gosalbes, B. Charlot, et A. Giani, « First high-g measurement bythermal accelerometers », in 2011 16th International Solid-State Sensors, Actuators and MicrosystemsConference, Beijing, China: IEEE, juin 2011, p. 84-87. doi: 10.1109/TRANSDUCERS.2011.5969142.

Acknowledgement: ANR-22-PEEL-0002, the French RENATECH network and Nanofutur.

COMPTERA

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4 Non-equilibrium carrier dynamics in HgTe quantum dots revealed by mid-infrared pump-THz probe spectroscopy

Colloidal semiconductor nanocrystals (NCs) exhibit unique optical and electronic properties, making them ideal candidates for many applications spanning the visible to mid-infrared spectral range. Among them, mercury telluride (HgTe) NCs are emerging as promising active quantum materials for THz applications. Notably, we have demonstrated a broad absorption resonance centered ~4.5 THz resulting from multiple intraband transitions of single carriers between quantized states [1, 2]. Also, recent studies have reported a coherent THz emission from large HgTe NCs excited by femtosecond optical pulses via second-order nonlinear effects, driven by both photogalvanic and photon drag mechanisms [3].
Here we investigate the non-equilibrium carrier dynamics at low energy in large HgTe NCs using mid-infrared pump-THz probe experiment. We report on carrier lifetime as long as >15 ps and examine the dependance of carrier recombination times on photocarrier density, revealing a square root scaling behavior. By exploring the underlying fundamental mechanisms of recombination, we evidence that Auger recombination is not relevant in this system, nor is the recombination process to direct energy transfer from the electronic transition to the ligand vibrational modes. Also, nonradiative recombination assisted by surface traps does not entail a square-root law with photocarrier densities, nor the radiative recombination process. The influence of lattice temperature on hot carrier dynamics further highlights the role of electron-phonon interactions in the recombination process. Furthermore, we observe a remarkably high photoinduced absorption of up to 30%. Our findings pave the way for the integration of large HgTe NCs in THz detectors, modulators, emitters, and quantum THz devices.

References:
[1] N. Goubet et al. J. Am. Chem. Soc., 140, 5033 (2018).
[2] T. Apretna et al. Nanophotonics, 10, 2753 (2021).
[3] T. Apretna et al. Appl. Phys. Lett. 121, 251101 (2022).

Acknowledgement: ANR-22-PEEL-0003

COMPTERA

Victor Merupo[1], D. Gacemi[2], P. Balla[1], J-F. Lampin[1], C. Sirtori[2], E. Peytavit[1], and S. Barbieri[1]

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5

Ultra-fast quantum-well mid-infrared photodetectors: time-resolved photocurrent and optical saturation by femtosecond laser excitation

AlGaAs/GaAs multi-quantum-well mid-infrared (MIR) photodetectors based on patch-antenna resonators have recently demonstrated unprecedented response times at room temperature [1, 2]. In this work we study their photoresponse in the time domain and their saturation properties, by illuminating detectors operating at 8μm wavelength with ~150fs optical pulses generated by a MIR comb oscillator. The generated photocurrent pulses are measured using a 67GHz bandwidth real-time oscilloscope. As shown in the figure, while the rise time is independent from the applied bias, the pulse decay shows significant changes. Depending on the bias conditions we observe pulse durations in the 10-25ps range, i.e. 3dB cutoffs of 15-25GHz. From impedance measurements under bias using a VNA analyzer we infer that the observed frequency response is not limited by the device parasitics but rather by the intrinsic dynamics of the photoexcited electrons. Results of optical saturation measurements in both pulsed and CW operation will also be presented and compared.

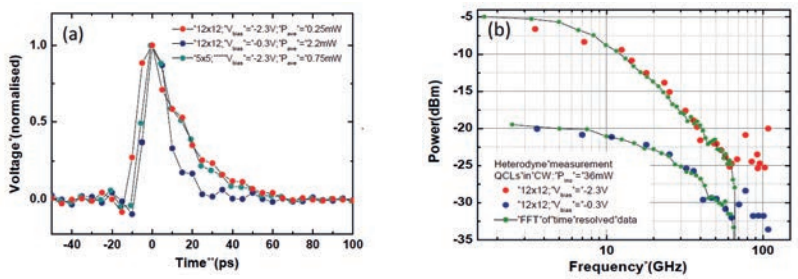

Fig.1 (a) Photocurrent pulses measured with a real time oscilloscope from two photodetectors based on 12x12=144 and 5x5=25 2D-arrays of patch-antennas. (b) Frequency response of the 12x12 device measured by heterodyning two quantum cascade lasers operated in CW (red and blue dots). Fourier transforms of the pulses in panel (a) (green dots).

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Acknowledgement: ANR-22-PEEL-0003

L'ÉLECTRONIQUE POUR LA CONVERSION

Projet VERTIGO

LTM | LAAS | CRHEA | IEMN | CEA-Leti | AMPERE | G2Elab | LAPLACE

VERTIGO vise à développer des transistors de puissance en Nitrure de Gallium (GaN) à géométrie verticale. Actuellement, ces transistors ont une structure latérale, ce qui limite leur tension de fonctionnement. La géométrie verticale permet de gagner en densité de courant, et la montée en tension (le projet vise 1200 V, avec des puces d'un calibre de 50 A) est obtenue avec des couches plus épaisses. Enfin, la montée en fréquence est permise par les mobilités importantes (objectif x10 par rapport aux résultats publiés) que le projet visera en travaillant sur le canal de conduction et en exploitant toute la richesse des hétérostructures AlGaN. Le projet utilise des couches épitaxiées sur saphir et silicium. Le retrait partiel ou total du substrat et le report sur un radiateur efficace permettront de gérer les problèmes électriques et thermiques de façon indépendante et flexible, pour proposer des solutions de packaging innovantes.

Projet OFCOC

FOTON | INL | C2N | CEA-Leti | IES

Les peignes de fréquences optiques ont un potentiel applicatif considérable dans les domaines de la santé, de l'environnement, de la sécurité ou des technologies de l'information. Très récemment, les premières démonstrations de peignes de fréquences sur puce (microcombs) ont ouvert la voie à leur utilisation future dans notre vie quotidienne, au sein de détecteurs de virus portables, de capteurs autonomes scrutant la qualité de l'air... sans parler des applications industrielles, spatiales et de défense. Avec le soutien de plateformes technologiques matures de la photonique silicium (Si, SiGe et SiNOI), **l'objectif d'OFCOC est la co-intégration de deux filières d'excellence françaises : les lasers à cascade interbande à base d'antimoine et la plateforme non-linéaire GaP, afin de réaliser la première source microcomb intégrée, large bande, robuste, fiable et miniaturisée sur une plateforme entièrement semi-conductrice.**

Projet FUN-TERA

C2N | XLIM | IETR | IEMN | CEA-Leti | LERMA

Depuis quelques années, on assiste à une accélération de la montée en fréquence des systèmes électroniques. La gamme 'térahertz', qui se situe au-delà de 200 GHz offre de nouvelles opportunités applicatives (communications haut-débit, radio-astronomie,...). Par exemple, les systèmes de communication THz nécessitent des émetteurs puissants, des détecteurs sensibles et large bande. Pour ces systèmes, il n'existe pas encore de filière française structurée. Nous disposons, en France, d'un tissu d'acteurs académiques reconnus pour la fabrication de sources et détecteurs à semi-conducteurs et leur utilisation pour des démonstrateurs THz (applications sus-citées). **Le projet FUN-TERA vise à structurer la communauté autour de ces composants unitaires et leur fonctionnalisation en vue d'applications.**

Projet GOTEN

GeMAC | INL | INSP | AMPERE | CEA-Irig | LGP | IEMN

GOTEN vise à démontrer la faisabilité d'une filière technologique française de composants verticaux à base d'oxyde de gallium (Ga_2O_3), couvrant l'ensemble de la chaîne de valeur allant de la croissance par épitaxie jusqu'à la gestion thermique des composants dans leur boîtier. Le dispositif ciblé est une diode p-n verticale basée sur une hétérostructure NiO/Ga_2O_3 assurant une tenue en tension de 10 kV et un courant élevé (> 10 A) en mode passant associés à un packaging spécifique.
Le Ga_2O_3, matériau à très grande bande interdite (4,8eV) est disponible à faible coût et en grande surface (> 150 mm). Bien qu'ayant une thermique 5 à 10 fois plus faible que le SiC ou le GaN, le Ga_2O_3 présente une très faible énergie d'activation du dopant (30meV), un champ critique (MV/cm) x4 par rapport au GaN ou SiC, et un BFOM (figure de mérite de l'électronique de puissance) un ordre de grandeur supérieur au SiC ou GaN.

Projet FRENCHDIAM

AMPERE | LAAS | GeMAC | Néel | CEA-Leti | LAPLACE | LSPM | CTReg

FRENCHDIAM cherche à exploiter les propriétés exceptionnelles du diamant, telles que sa tenue aux champs électriques importants, sa résistance à des températures élevées et sa conductivité thermique exceptionnelle. **Le projet vise à démontrer la faisabilité de deux dispositifs avancés complémentaires en diamant : un transistor vertical haute tension et une cellule de commutation monolithique.** Diverses étapes technologiques nécessaires pour une filière de production seront développées comme la croissance des substrats de grande taille, l'épitaxie de couches dopées, la structuration en salle blanche, la protection périphérique et la conception d'une électronique de commande. FRENCHDIAM mettra aussi l'accent sur l'évaluation de l'impact sur l'environnement de la fabrication de composants en diamant.

Projet NANOFILN

FEMTO-ST | LAAS | INPHYNI | C2N | CEA-Leti

NanoFILN a pour objectif de mettre en place une filière technologique nationale amont (réseau RENATECH et CEA), pour les composants en optique intégrée de nouvelle génération basés sur l'utilisation de films minces de $LiNbO_3$. Deux démonstrateurs exploitent les propriétés remarquables du $LiNbO_3$. Le premier utilise l'effet électro-optique (modulateur/switch) tandis que le deuxième se base sur l'effet non-linéaire (générateur de photons jumeaux). Nous nous concentrons sur l'intégration de fonctions multiples sur puce monolithique et l'hybridation sur silicium. L'accès simultané à trois méthodes complémentaires d'élaboration des films minces (100 nm – quelques μm) de $LiNbO_3$: la découpe ionique, le report, l'amincissement et l'épitaxie, est unique au niveau mondial. Les deux applications cibles concernent le domaine de l'optique quantique et des télécoms, mais il est évident que le savoir-faire développé sera aisément transposable à d'autres domaines (analyse environnementale, traitement du signal, ...)

VERTIGO

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6 Design of gallium nitride (GaN) power devices and functions for high voltage applications

Efficient energy management is one of the most critical challenges of the 21st century, driving the need for advanced power switching technologies to minimize energy losses and improve performance. Wide bandgap semiconductors such as gallium nitride (GaN) have emerged as promising candidates for nextgeneration power devices due to their exceptional intrinsic properties. However, existing GaN devices, which are predominantly lateral AlGaN/GaN heterostructures, face several limitations. These include low threshold voltage, restricted breakdown voltage, high dynamic on-resistance, and trade-offs between breakdown voltage and power density, which hinder their use in high-power and high-voltage applications. To address these challenges, our research work focuses on the development of vertical GaN power devices capable of achieving high breakdown voltages with a minimal surface footprint. The first part of the work is the design of '1200 V breakdown voltage / 1 m $\Omega.cm^2$ specific on-resistance' vertical GaN MOSFETs, by proposing and optimizing devices architectures (doping concentrations and dimensions of the layers — especially the epitaxial layers —, trench dimensions — width, depth —, etc.). The second part of the work is exploratory: we propose to study original vertical GaN structures (Superjunction MOSFET, FinFET and IGBT) using 2D and 3D simulations and then, as already done in the past for silicon devices, to develop a methodology for the design of GaN power functions targeting, for example, the production of fully integrated converters. This research aims to advance the state-of-the-art in vertical GaN power devices, contributing to the development of energy-efficient and reliable power systems for the future.

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VERTIGO

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7 Conception d'un convertisseur de puissance utilisant des composants de puissance GaN verticaux

Dans le cadre du projet VERTIGO [1], différentes problématiques CEM, thermiques, électriques et technologiques liées à la conception d'un packaging pour une puce semi-conductrice verticale en GaN sont étudiées. En ce qui concerne la compatibilité électromagnétique, sans un packaging adapté, les forts $\frac{dv}{dt}$ et $\frac{di}{dt}$ des puces GaN engendrent des perturbations CEM conduites. Les capacités parasites de mode commun entre la phase et le dissipateur ou encore les inductances parasites dues à la longueur des pistes crées courants et surtensions perturbant le composant de puissance et son environnement. Nous travaillons sur la conception d'un packaging minimisant les perturbations CEM. Pour ce premier prototype, des transistors MOSFET Si à structure verticale sont utilisés [2]. Ces puces ont des caractéristiques différentes des puces GaN verticales de VERTIGO, mais cependant leur structure verticale et leur vitesse de commutation élevée est représentative du comportement CEM des puces GaN verticales. Ce prototype sert avant tout à mettre en place le concept de maitrise des perturbations CEM pour un packaging de transistor à structure verticale. Le packaging conçu est constitué de deux circuits imprimés double couche entre lesquels sont brasés deux transistors Si formant la cellule de commutation. Les écrans à potentiels fixes de part et d'autre des puces permettent de minimiser les capacités parasites. La disposition des puces en flip-chip réduit la maille de commutation et permet de diminuer les inductances parasites. Le dispositif est conçu pour dissiper la chaleur de façon identique pour chaque puce. Enfin, l'adaptation de ce packaging à un transistor GaN vertical ou à une puce de caractéristiques proches [3] est un point à travailler dans la suite du projet.

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VERTIGO

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8 Growth and characterization of thick epitaxial GaN layers for power electronics applications

The PEPR VERTIGO project aims at elaborating thick epitaxial GaN layers (> 5 µm) for vertical transistors exhibiting breakdown voltages ≥1,2 kV and direct currents ≥50 A. In order to achieve these goals, the epitaxial layers must display a uniformly low biaxial stress, a low dislocation density and a uniformly low n-carrier density [1], [2]. Due to the difficulties in growing thick GaN layers on silicon wafers [2], with a low dislocations density, we report in this work the synthesis and the physical and electrical characterizations of thick n-GaN layers grown by MOCVD on sapphire substrates. These layers will be eventually transferred onto silicon substrates. Physical characterizations show that these layers display similar crystalline structure, regardless of the doping concentration (1.4 – 5.5 10^{15} cm^{-3}), as expressed by the XRD, AFM, SEM, Raman spectroscopy and C-V measurements results. Schottky barrier diodes (SBDs) fabricated on the n-GaN layers are then electrically characterized through forward and reverse current measurements. Most SBDs have similar ideality factors, Schottky barrier height values and reverse current densities. Surface defects negatively impact diodes turn-on voltages and specific on-resistances (9 – 20 $m\Omega \cdot cm^2$), while some peculiar defects are found to be highly detrimental to reverse current characteristics. Most diodes display specific on-resistances and reverse current densities comparable to some of the best vertical GaN-based SBDs [3], [4], which may be due to the uniformity of the n-doping concentration and the low density of screw-type dislocations. Breakdown voltage measurements are in progress.

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VERTIGO

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9 Pseudo-vertical GaN-on-Si trench-MOSFETs for power applications

Over recent years, vertical GaN-based transistors have demonstrated increasing potential for efficient power switching applications due to their high voltage and high current handling capability. Different vertical GaN technologies demonstrating high-performances have been successfully fabricated on GaN substrates primarily, with among them, the conventional GaN trench-MOSFETs. However, the high cost and limited size of low-defect-density GaN substrates have limited the scaling of volume production. As a more cost-effective platform, GaN-on-Si has been explored for GaN vertical devices [1-3], paving the way for the development of more cost effective high-performances GaN-on-Si trench-MOSFETs. Consequently, we present the process development of pseudo-vertical GaN-on-Si trench-MOSFET test structures. Overall, transistors show promising ON-state performances : 1) a normally-OFF (V_{th} ~ 4 V) behaviour, 2) adequate switching capabilities (high I_{ON}/I_{OFF} of ~10^8, subthreshold slope of ~240mV/dec), 3) significantly small gate leakage current (10^{-11} A). These promising preliminary test structures act as a milestone for future gate module optimization on GaN-on-Si vertical trench-MOSFETs.

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VERTIGO

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Fully-vertical GaN-on-GaN trench-MOSFETs for power applications

Over recent years, vertical GaN-based transistors have demonstrated increasing potential for efficient power switching applications due to their high voltage and high current handling capability. Among the technologies that are still under development, the well-known vertical power trench-MOSFET shows much potential regarding the benefits of the MOS gate technology. Nowadays, high-performance GaN trench-MOSFETs have been successfully demonstrated based on bulk GaN substrates [1-3]. These vertical devices act as reference test structures to pursue the optimization of the device process fabrication.
Thus, in this work, fully-vertical GaN trench-MOSFETs were fabricated and electrically characterized to evaluate their ON-state performances. Transistors show a normally-OFF behaviour (Vth ~1 V) with adequate switch capabilities (high I_{ON}/I_{OFF} ratio of ~10^9, adequate subthreshold slope of ~139mV/dec) and significantly small gate leakage current (10^{-11} A/mm). An improved resistance partitioning method is also introduced [4], which enable an accurate extraction of the resistances of the trench bottom and trench sidewalls by taking into account different charging conditions. This methodology enabled an estimation of the effective sidewall and bottom mobilities of 11.1 $cm^2/V.s$ and 15.6 $cm^2/V.s$, respectively. These ON-state performances are promising, and act as starting point to be improved upon thanks to the optimization of the gate module of our fully-vertical MOSFETs;

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VERTIGO

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11

Towards novel GaN on silicon fully vertical MOSFET for high power energy conversion

Lateral GaN devices face significant limitations for high voltage (>650V) power applications, including excessive device footprint, reliability concerns related to surface and bulk traps, and the absence of avalanche breakdown. To overcome these challenges, the development of vertical GaN devices has gained momentum and is being extensively studied globally. State-of-the-art vertical GaN devices are typically fabricated on bulk GaN substrates, which provide superior quality due to low dislocation density and low impurity levels. However, these substrates are prohibitively expensive and available only in small areas, hindering broader adoption. By employing heteroepitaxial growth of GaN on substrates such as silicon or sapphire, manufacturers can significantly reduce production costs and limited availability of native GaN wafers. The fabrication of vertical GaN power transistors on alternative substrates has emerged as a cost-effective and efficient solution to high-efficient components.
Recent advancements include achieving a 1200 V breakdown voltage in quasi-vertical diodes on both silicon and sapphire substrates. Additionally, the successful development of a fully vertical transistor [1] marks a significant milestone. This demonstrator features application-relevant transistor areas and full 150 mm wafer processing within a manufacturing-compatible flow. Despite these breakthroughs, key challenges remain such as achieving area-selective p-type doping via implantation, which is crucial for ensuring adequate shielding in power transistors.
This presentation will provide a comprehensive overview of the current landscape of vertical GaN power transistors, highlighting major achievements and discussing the key issues that must be resolved to enable further technological advancement.

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OFCOC

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12 Sources non linéaires moyen infrarouge sur plateformes photoniques Silicium/germanium

Des efforts considérables ont été déployés récemment pour intégrer complètement les fonctions moyen infrarouge (MIR) sur puces à base de germanium Ge, et ceci dans le but d'accroître la fiabilité, d'améliorer les performances et de réduire les coûts pour une large gamme d'applications [1]. La source lumineuse est un composant essentiel des systèmes intégrés de spectroscopie MIR. Nous examinons ici les avancées récentes dans la génération de sources de lumière supercontinuum avec des plateformes photoniques MIR basées sur des couches épaisses de Ge [2] (figure 1a) et de silicium germanium SiGe sur du silicium Si [3](figure 1b), incorporant éventuellement du silicium nitrure SiN entre les couches (figure 1c). Unsupercontinuum brillant et large couvrant 1,4 octave entre 3.5 µm et 8 µm avec une puissance moyennede 20 mW a été généré sur la plateforme $Si_{0,6}Ge_{0,4}$/Si [3], tandis qu'un supercontinuum d'une octave entre 3.39 to 6 µm a été obtenu sur les plateformes Ge/Si [2]. Pour des applications nécessitant une cohérence élevée, il est possible de générer des supercontinuums cohérents, un supercontinuum d'une octave entre 2.8 µm et 5.7 µm est généré en régime de dispersion normale dans des guides d'ondes à base de silicium germanium [4]. Les guides d'ondes à base de Ge offrent donc un niveau de flexibilité important pour gérerla dispersion, exacerber les effets non linéaires de la lumière dans les guides d'ondes (figure 1d/e) etminimiser les puissances maximums des pompes.

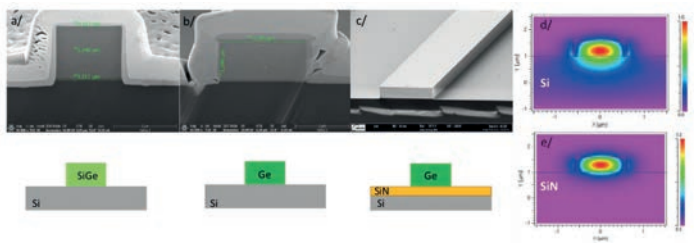

Figure 1: Image de microscopie électronique (a) d'un guide d'ondes $Si_{0,6}Ge_{0,4}$/Si clivé, (b) d'un guide d'ondes Ge/Si et (c) d'un guide d'ondes Ge/SiN. Profil du champ électrique (d) d'un guide d'ondes Ge/Si et (e) d'un guide d'ondes Ge/SiN.

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OFCOC

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13 Résonateurs en anneaux intégrés à facteur de qualité d'un million dans l'infrarouge moyen

La photonique dans l'infrarouge moyen (MIR), qui englobe la gamme de longueurs d'onde d'environ 3 à 15 µm, a suscité une grande attention en raison de son importance dans de nombreux domaines [1]. Une multitudes plateformes différentes ont été proposées et étudiées pour le MIR. Les matériaux photoniques du groupe IV, tels que les alliages de silicium et de germanium (SiGe), constituent une classe très prometteuse [2]. Un élément fondamental et important des circuits intégrés photoniques (PIC) est un résonateur compact capable de confiner efficacement la lumière, c'est-à-dire avec un facteur Q de haute qualité [3]. Les micro-anneaux sont essentiels dans les PIC pour la conception de filtres optiques, de modulateurs et de traitement des signaux optiques [4]. Dans ce travail, nous démontrons une amélioration significative du facteur Q des résonateurs annulaires $Si_{0.6}Ge_{0.4}$/Si vers un million autour de 4 µm de longueur d'onde, ce qui constitue un record pour la photonique du groupe IV. Ce résultat a été obtenu grâce à un processus de fabrication optimisé. Nous effectuons une analyse de la distribution statistique des facteurs Q entre une partie relativement large (3.5-4.6 µm) de la bande MIR. Avec un facteur Q d'un million, SiGe/Si devance les autres plateformes photoniques MIR intégrées dans la quête d'un Q élevé.

Figure 1: (a) Image de microscope électronique à balayage montrant le gap de 250 nm entre un résonateur en SiGe/Si et son guide d'accès, aux dimensions de 3.5 x 3.5 µm. (b) Mesures du facteur de qualité Q pour un résonateur en $Si_{0,6}Ge_{0,4}$/Si avec un gap de 500 nm et pour dimension 3.5 x 5 µm.

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Gallium Phosphide platforms for integrated photonics

Gallium Phosphide (GaP) is a III-V semiconductor with many advantages for integrated non-linear photonics such as a wide transparency band (visible, NIR, MIR) pushing the absorption threshold to two photons below 1100 nm, a high refractive index ($n_0 > 3$), an indirect gap, and large nonlinearities at the second and third-order ($n_2 = 1.2 \times 10\text{-}17$ m²/W [1]). GaP photonic devices can be produced from the growth of GaP on different substrates like Gallium Arsenide (GaAs) [2], Silicon (Si) [3] or on native substrates [4]. In this work, we investigate the impact of the photonic platform used on the propagation losses of GaP nano-waveguides and evaluate their relevance in the development of advanced GaP photonic circuits. Propagation loss measurements using the Fabry-Perot contrast method [5] are presented and we demonstrate state state-of-the art performances for GaP photonics based on GaAs substrates. We also discuss the properties of microring resonators and first nonlinear characterizations in the context of frequency comb generation.

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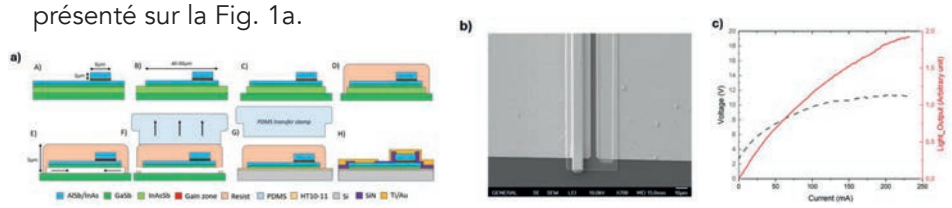
Intégration par Micro-Transfer-Printing de lasers à cascade interbande sur Si

La génération de peignes de fréquences optiques dans la gamme de l'infrarouge moyen (MIR), couvrant des longueurs d'onde de 3 à 15 µm, offre des perspectives intéressantes pour le développement de diverses applications telles que la spectroscopie, la surveillance environnementale, la médecine et la défense [1]. Cependant, le coût élevé et la complexité des équipements nécessaires à la mise en oeuvre de ces peignes limitent actuellement leur utilisation aux laboratoires. Intégrer un laser à cascade interbande (ICL) [2] de pompe sur une plateforme où l'effet Kerr génère de nouvelles fréquences optiques [3], permettrait de réduire considérablement la taille et la consommation d'énergie de la génération de peignes de fréquences.
Parmi les différentes approches d'intégration de sources laser à semi-conducteurs sur une plateforme photonique en silicium, le transfert de coupons laser par micro-transfer printing (µTP) représente une alternative avec des avantages uniques, notamment la possibilité d'effectuer les premières étapes de fabrication des lasers sur leur substrat d'origine [4]. Le procédé technologique développé pour la réalisation des ICLs sur silicium via µTP est présenté sur la Fig. 1a.



Les premiers transferts d'ICL ont été démontrés avec succès sur une cible en silicium. Un dispositif typique est présenté sur la Fig. 1b. Les courbes PIV (Fig. 1c) montrent une injection de porteurs réussie dans le dispositif µTP ainsi qu'une émission lumineuse. Cependant, la tension de seuil et la résistance série sont élevées, ce qui empêche l'action laser avec ces dispositifs préliminaires. Des travaux sont en cours pour résoudre ces problèmes. La formation d'une cavité hybride avec une plateforme photonique en Si ou SiGe est également prévue.

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16

Polycrystalline zinc sulfide waveguides for second order nonlinear integrated photonics

Zinc Sulfide (ZnS) holds significant promise for integrated second-order nonlinear optics, particularly due to its high bandgap energy. Although ZnS offers a high refractive index [1], broad transparency, and substantial nonlinear coefficients [2], [3], its potential in integrated nonlinear photonics remains underexplored. Here, we investigate the structural and optical properties of ZnS thin films deposited via magnetron sputtering, demonstrating their suitability for advanced photonic applications. The fabrication and characterization of waveguides based on ZnS are presented, along with theoretical analyses of possible nonlinear processes in such polycrystalline material. These findings are supported by second harmonic generation experiments, highlighting ZnS's potential as a key material for next-generation photonic technologies.

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17

Fabrication and Characterization of Transverse Orientation-Patterned Gallium Phosphide Nanowaveguides for Second Harmonic Generation

Thanks to its intrinsic properties, such as its high non-linear coefficients of order 2 and 3 and its wide transparency range (0.5 - 12 µm), gallium phosphide (GaP) is of particular interest in integrated photonics. To use this material in the context of spectral conversion driven by second order processes, achieving a phase-matching condition between interacting waves within it is key. One way of achieving that condition can be obtained through a periodic modulation of the material nonlinear response along the propagation direction. This technique, known as quasi-phase-matching (QPM), has enabled high efficiencies second harmonic generation (SHG) in orientation-patterned gallium phosphide (OP-GaP) integrated guided structures, at the cost of more complex fabrication process [1]. An alternative approach consists of modal phase matching (MPM) [2], which generally present low mode overlap that negatively impacts the SHG efficiency. In the last decade, some works proposed innovative nonlinear waveguide designs that involves the vertical control of the material susceptibility, enabling MPM configurations previously constrained by selection rules, resulting in improved mode overlaps [3-4].
In this work, we present the first demonstration of high-efficiency SHG in transverse orientation-patterned gallium phosphide (TOP-GaP) nanowaveguides, using modal phase-matched TE00 pump mode and TM10 second harmonic mode. The underlying principle of TOP-GaP waveguides, along with their fabrication and characterizations, will be discussed in detail.

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18 Embedded optimization of 90° Hybrid couplers in power combined frequency doublers

At the Observatoire de Paris we develop Schottky multipliers mostly for local oscillator chains, that are essential for heterodyne receivers, which are widely used in far infra-red radio-astronomy, where a spectral resolution of 10^6 or better is required. The goal frequency of 1.9 THz (task 3.3 of the project FUNTERA) corresponds to the very important line of [CII] opening a window for studies of star formation, black hole feeding, and other phenomena. Intermediate frequency Local Oscillators (LO) at 345 GHz THz are also necessary for observations of the CO J=3-2 transition, which allow astronomers to understand how stars and planets form. Powerful LOs (1 mW at 1.9 THz) can be used to pump large heterodyne arrays to efficiently map large areas of molecular gas. These sources are based on power combined multiplication elements driven by high power amplifiers at W-band or above [1, 2]. To fulfill our output power goal, we need to extend power combing structures. The number of elements is usually limited to 2 or 4, often optimized separately. In order to increase this number significantly, we need to keep the phase and amplitude imbalance between each branch at minimum while matching the impedance across the frequency range. In this study, we investigate on the optimization of a 90° hybrid coupler when it is embedded at the input of the frequency multiplier elements. We realize a lumped-model version of a 90° hybrid [3] that is embedded in a 2-way power combining doubler at 345 GHz, adapted from [4].

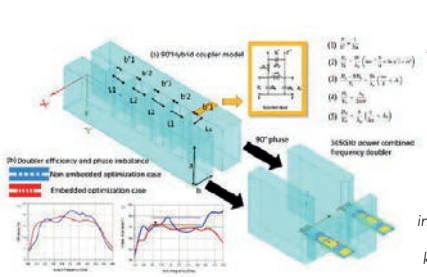

Fig. 2 (a) Electrical model of 90° hybrid coupler implemented in KeySight ADS using RWG electrical model transitions. In this illustration, the Hybrid model has a symmetry along zy plane. b' and L are the dimension variables and are fed in the impedance/admittances lumped model through equations 2,3,4, 5. The hybrid model is optimized in a conjoint simulation with a 2-way frequency multiplication scheme at 345 GHz, (b) Example of phase imbalance improvement and full architecture efficiency for Non embedded optimized hybrid case - in blue - and Embedded optimized hybrid case - in red-.

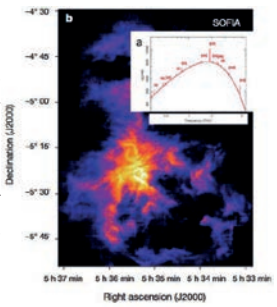

Fig. 1 (a) Schematic of the spectral characteristics observed toward an interstellar cloud, featuring a 30 K continuum, an assortment of selected atomic and molecular spectral lines. From Kulesa2011. (b) The integrated 1.9-THz (158-μm) [C ii] emission, observed by the upGREAT instrument on board SOFIA, traces the cooling and kinematics of the gas in the photodissociation region. From Pabst2019 et al.

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19 Micro fabrication techniques for sub-THz antennas

Terahertz (THz) and sub-THz communications are extensively studied for their large available bandwidth, enabling high data rates (over 100 Gbps) with low latency. To make the most of such large bandwidths, one has to compensate the free space path loss (FSPL), which is proportional to the square of the carrier frequency and typically burdens the link budget as one approaches sub-THz bands. Sub-terahertz antennas must therefore feature large collecting areas to counteract the high propagation losses. The short wavelength also demands high accuracy and tight tolerances on electrically large surfaces.
To address these challenges, we have explored different patterning and etching techniques (e.g., photo/maskless lithography, chemical and Bosch etching processes) as well as different substrates (e.g. quartz, silicon, cyclic Olefin copolymer (COC)). Applications include multi-layer frequency selective surfaces (FSSs) [1], Luneburg Lens Beamformers (LLBs) [2] and modulated metasurface (MTS) antennas [3].
FSS devices were fabricated on 200 μm thick quartz substrates by Al lift off process (x3). Processing such thin substrates can be challenging, as is front/back side photoalignment with 2 fused quartz substrates. For the LLB device, it was made on a COC substrate using a photolithography-chemical etching process. Substrate-related constraints, such as process temperatures and layer deposition parameters, must be carefully considered to avoid its deformation. Finally, modulated MTS antennas are fabricated on Si wafers using deep plasma etching (Bosch process) to pattern both the front and back sides. Extensive optimization is needed to achieve straight features over large depths (200 μm), ensuring good match between the designed and fabricated patterns.

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20 Micro Additive Manufacturing for High-Precision Micro-Interconnections in RF Systems

Micro additive manufacturing (μAM) of metals provides us with a modern and futuristic approach for fabricating high-precision micro-interconnections in RF systems. By enabling the creation of complex 3D geometries with micron-scale resolution, with μAM we want to bridge the gap between different electronic components, such as chips and packages, in high-frequency applications. This technique allows us to localize an electrodeposition process using an atomic force microscope (AFM) cantilever tip, achieving printing resolutions in the order of ~2 μm and sub-micron alignment accuracy [1].
One of the key advantages of μAM is its ability to fabricate overhanging structures without requiring support materials, simplifying the manufacturing of intricate 3D architectures [2]. Compared to conventional microfabrication techniques, μAM provides enhanced design flexibility, while maintaining excellent surface quality, which is needed to have a better performance in terms of signal quality and efficiency. By leveraging advanced techniques in micro additive manufacturing, we will attempt to optimize the precision of interconnections while minimizing potential failure points.
This research aims to refine μAM techniques for reliable, high-performance micro-interconnections, addressing key challenges such as geometry accuracy, alignment precision, and material compatibility with semiconductor packaging.

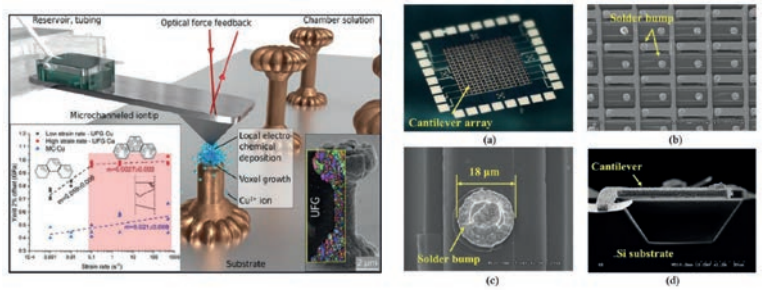

Fig. 1. Left: principle of the micro electrochemical additive manufacturing (© Exaddon); Right: example of current micro-cantilever using MEMS technology that we want to mimick using micro-3D printing [3]

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21 Photonic Emitters Based on Photomixing Antenna Arrays for Directional Power Combining

To address the exponential increase in mobile data traffic, new ultra-high-speed wireless technologies must be developed. Achieving data rates exceeding 100 Gbits/s will require the use of very high carrier frequencies to fully exploit the wide bandwidth available in this spectral region. The 2023 World Radiocommunication Conference resolution COM6/17 has identified several sub-THz bands for the development of the next generation of mobile communications. This thesis aims to leverage the D-band (110 GHz – 170 GHz) and H-band (220 GHz – 330 GHz) sub-THz frequency windows to achieve such real-time data rates.
On one hand, developing new room-temperature, wideband sources (e.g., photodiodes) to increase the power generated in the THz gap is essential for compensating free-space propagation losses while fully exploiting the available bandwidth [2]. On the other hand, for effective use in field wireless applications, the generated signals must be transmitted only in the directions where they are needed. To achieve this, narrow, highly directional, and steerable beams must be generated across a sufficiently wide field of view [3]. We will explore the integration of UTC photodiodes (IEMN) with wideband planar antenna arrays (IETR), matched to the UTC impedance [4]. The antenna arrays, developed and excited by photomixing, will rely on coherent power combination to enable beam steering. By controlling the phase of each radiating element through photonic beamforming, it will be possible to direct the radiation in a preferred direction. The goal is to propose sub-THz photonic antenna arrays that surpass the current state of the art in performance.

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GOTEN

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22 Vertical p-NiO/n-Ga_2O_3 Heterojunction Diodes for High Power Applications

The industrial development of wide bandgap semiconductors, particularly GaN and SiC, is advancing rapidly, with applications extending beyond the 600 V/1200 V range into high-voltage nodes (>3 kV) for power conversion. Gallium oxide (Ga_2O_3), an UWBG material, has significant attention due to its exceptional material properties, including a large bandgap enabling high-temperature operation and a high breakdown field supporting high-voltage performance. Ga_2O_3 offers potential advantages over SiC and GaN in power device performance and cost-effectiveness, making it a promising candidate for next-generation high-power and high-temperature electronics.
This work focuses on developing a vertical p-n diode based on a NiO/Ga_2O_3 heterostructure, targeting a breakdown voltage of 10 kV and high on-state current (>10 A). Using Silvaco TCAD simulations, we compare the electrical performance of NiO/Ga_2O_3 p-n diodes with Ga_2O_3 Schottky diode. Defining Ga_2O_3 and NiO in the simulation was challenging but critical to obtaining accurate results.
The simulated Ga_2O_3 Schottky diode demonstrated a breakdown voltage of 1083 V at 1×10^{-3} A, with an on-state current of 1.6 A at 5 V and low on state voltage drop. Schottky diode exhibit device temperature of 576 ˚C at 5 V, which shows a poor heat dissipation in Ga_2O_3 diode. Conversely, the NiO/Ga_2O_3 p-n diode exhibited a breakdown voltage of 1980V at 1×10^{-6} A, an on-state current of 1.4 A, and device temperature of 503 ˚C, showing poor heat dissipation but better than Schottky diode.
These results demonstrate the NiO/Ga_2O_3 p-n diode enhanced performance, including higher breakdown voltage, lower leakage current, and better heat dissipation, making it a superior choice for high-power applications.

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23 Design, fabrication and characterization of new Ga_2O_3-based power devices for high voltage conversion

In addition to the 600 V/1200 V applications covered by Wide BandGap (WBG) materials, other technological targets exceeding 3 kV align with existing markets for High Voltage (HV) conversion and protection. These include electricity distribution, SMART grids, onshore wind (3.3 kV) offshore (6.5 kV), rail transport, and charging electric vehicles from HV (22 kV) lines.
Three Ultra-Wide BandGap (UWBG) materials have been gaining significant attention for HV devices. Among these materials, and also considering both GaN and SiC, Gallium Oxide (Ga_2O_3) stands out as the only one that can be produced via liquid phase using conventional drawing processes.
The potential performances of Ga_2O_3-based devices in power electronics surpasses that of other WBG and UWBG materials, highlighting its promise for very high-power applications. In addition, an anticipated reduction in the cost of 6-inch substrates to $300 in 2030 is expected to make Ga_2O_3 more accessible.
This project focuses on the design and development of these components using TCAD Silvaco tools. It will include the fabrication of test vehicles for rapid material optimization, as well as the fabrication of a targeted device and the associated electrical characteristics. The primary objective is to create a diode delivering a breakdown voltage of 10 kV and a high current in on state (>10 A), combined with a tailored packaging solution. The initial phase of this project involves testing and optimization etching processes for Ga_2O_3. Subsequently, Schottky diodes will be fabricated and characterized as a precursor to the development of PiN diodes incorporating p+ doped NiO.

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24 Conception, fabrication et caractérisation de transistors verticaux de puissance en diamant avec terminaison de jonction

Dans un contexte où la réduction des émissions de gaz à effet de serre est essentielle, la gestion de l'énergie électrique devient une priorité de premier plan, tant au niveau national qu'européen et international. Chaque maillon de la chaîne énergétique est impliqué dans cet effort pour diminuer l'empreinte carbone. Les méthodes de gestion, de transport et de distribution de l'énergie évoluent, avec l'introduction de smart grids et de réseaux HVDC, ce qui amène à réviser et repenser les convertisseurs électriques. Les composants de puissance jouent un rôle central dans cette transformation, favorisant l'émergence et la commercialisation de dispositifs fabriqués à partir de semiconducteurs à large bande interdite.
Le diamant (C), matériau à très large bande interdite, est connu pour ses propriétés thermiques et électriques exceptionnelles. Bien que pas encore mature du point de vue industriel, plusieurs études ont permis d'améliorer la maîtrise des niveaux de dopage possible et des preuves de concept ont permis de démontrer la viabilité de potentiels composants de puissance en diamant à destination des applications HVDC.
C'est dans ce contexte qu'un transistor vertical de type JFET en diamant sera développé, conçu pour supporter une tension de 3 kV, avec une terminaison périphérique offrant une efficacité minimale de 80% et une résistance spécifique de 10^{-2} Ω·cm².

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25 Fabrication et caractérisation de diodes Schottky diamant haute tension protégées par plaque de champ avec empilement Al_2O_3/Si_3N_4

Dans un contexte d'électrification des systèmes, l'optimisation des composants électroniques est primordiale pour réduire la consommation énergétique. Parmi les matériaux à large bande interdite étudiés pour remplacer le silicium, le diamant se distingue comme un candidat prometteur pour des applications de forte puissance.
À ce jour, la diode Schottky représente le dispositif en diamant le plus étudié et présente des résultats prometteurs. Toutefois, des améliorations demeurent nécessaires pour accroître la tension de claquage. L'absence de terminaison de jonction efficace provoque notamment une concentration du champ électrique en périphérie du composant, entraînant un claquage électrique prématuré, et limitant ainsi les performances des composants diamant.
La solution de protection périphérique par plaque de champ (Field Plate, FP) est couramment utilisée pour protéger le contact Schottky et réduire le champ électrique au bord de celui-ci. Cependant, l'emploi de matériaux à faible permittivité dans de nombreuses structures de FP est à l'origine d'un claquage prématuré du diélectrique, dégradant ainsi l'efficacité de la protection périphérique. Pour y remédier, nous proposons une configuration de FP basé sur un empilement Al_2O_3/Si_3N_4 (20/200 nm), présentant des permittivités élevées. La qualité de l'empilement a été préalablement étudiée par des mesures C-V sur silicium.
Le processus de fabrication des diodes sera présenté. La tension de claquage sera évaluée par des mesures I(V) réalisées dans un environnement sous vide entre 300K et 850K. Par ailleurs, la nature et la densité des pièges présents dans les diélectriques, pouvant altérer les performances des diodes, seront étudiées et caractérisées à l'aide de mesures C-V réalisées sur des capacités MIS (Métal-Isolant-Semi-conducteur) intégrées au même échantillon de diamant.

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26 Caractérisations innovantes de composants de puissance diamant pour des applications en électronique de puissance

La demande en énergie propre et efficace ne cesse de croître, qu'il s'agisse de véhicules électriques, de sources d'énergie renouvelable ou d'autres appareils électroniques. Par conséquent, le monde moderne exige le développement de technologies de conversion et de gestion de l'énergie toujours plus efficaces, fiables et durables. Dans le domaine de l'électronique de puissance, la technologie basée sur le diamant offre des avantages significatifs par rapport aux technologies à grand gap actuelles, telles que le GaN et le SiC. Cela justifie pleinement le développement et l'approfondissement de cette technologie. Dans le cadre de ce projet, les travaux de recherche s'appuieront sur les plateformes de test de puissance et de caractérisation additive du CEA Occitanie et du LAAS-CNRS afin de caractériser de manière approfondie des composants de puissance en diamant dans une optique de compréhension de leur fonctionnement et de leur impact sur leur environnement (packaging, application...) et réciproquement. Pour ce faire, nous ferons appel à des techniques expérimentales avancées permettant d'évaluer les pertes dans les composants, maîtriser leur pilotage et d'étudier les effets thermiques.
L'aspect de la gestion thermique et du packaging sera également abordé via l'impression de structures 3D céramiques afin d'étudier la réciprocité des effets entre le composant et son environnement proche.

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27 Heterogeneous growth and integration of $LiNbO_3$ films in acousto-optical components

$LiNbO_3$ (LN) is well known for its exceptional acoustic, electro-optic, pyroelectric and ferroelectric properties and has been extensively studied [1]. However, LN is not compatible with CMOS standard processes due to potential lithium contamination. Therefore, heterogeneous integration of LN is a solution to take advantage of the good electroactive properties of LN in the well-established and mature silicon platform. The aim of the NanoFiLN project in the frame of PEPR Electronics is to establish a national academic sector for a new generation of integrated optical components based on LN films. My thesis will focus on the heterogeneous integration of epitaxial thin film lithium niobate (TFLN) with silicon technologies and the coupling of TFLN with semiconductors for opto-mechanical devices. The direct liquid injection CVD technique has been successfully used to grow high quality epitaxial/textured LN films[2]. The first stage of the thesis involves growing stoichiometric LN on a sacrificial layer, which needs to be specified and optimised in order to develop the epitaxial layer transfer technique. The next steps will be to use the micro-transfer printing to integrate TFLN with photonic circuits and to couple them to other components.

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28 Design, fabrication and characterization of new Ga_2O_3-based power devices for high voltage conversion

Lithium Niobate (LN) is a key material for photonic devices thanks to its wide transparency window and its remarkable electro-optic and non-linear properties. More recently, through the ion slicing technique, Thin Film LN (TFLN) has become more available, leading the way into the development of higher-performance LN devices with a potential for densely integrated photonics chips. In this context, the NanoFiLN project funded by the PEPR-Électronique aims to establish a French technological sector for the development of optical chips based on LN films.
One aspect, in the frame of one starting thesis of the NanoFiLN project, is to develop key passive functions. Fiber-to-chip coupling still represents a fundamental challenge on TFLN platform due to the mode mismatch between the nanowaveguides and standard optical fibers [1]. An initial goal is thus to design and fabricate a light coupling device on TFLN with minimal loss and a simple fabrication technique, facilitating integration with other functions. The initial step of this study is to master the fabrication of the nanowaveguides on TFLN and accurately assess their propagation losses. First results will be exposed. Architectures of fiber-to-waveguide coupling will be proposed based on the state of the art as well as original solutions. To do so, simulations will be performed in parallel with the fabrication and characterization of guides and couplers. Then the study could extend to other passive functions trying to improve co-directional coupling or to minimize losses in bended waveguides, for instance.

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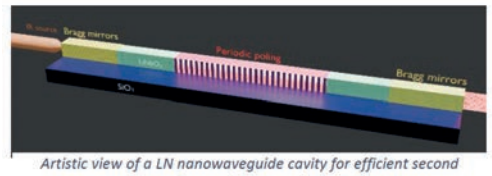
29 Second harmonic generation in a $LiNbO_3$ nanowaveguide cavity

Lithium niobate (LN) is a crystal known for its appealing optical physical properties, from its wide transparency window in the visible and mid-infrared to its high nonlinear coefficients. In the past decade, a renewed interest for this material has appeared worldwide in laboratories thanks to the development of thin film LN (TFLN), opening the path towards LN-based integrated photonics embedding various passive and active functions [1]. The NanoFiLN project aims at the implementation and development of a national academic sector dedicated to TFLN technologies, targeting monolithic integration of multifunctional chips.
In this framework, one goal is to develop TFLN structures to allow efficient nonlinear interactions at low power that would open up a wide range of applications from sensors to quantum optics and telecommunications. More specifically, a starting work is tackling second harmonic generation (SHG) in periodically poled nanowaveguides, enhanced with a resonant cavity as illustrated in the enclosed figure.
Up to now, separated tasks required for this advanced design have been demonstrated or are in progress. Ridge waveguides with nanostructured Bragg mirrors exhibited an extinction ratio above 20 dB at telecom wavelengths have been fabricated. First results on periodic poling of LN films have also been obtained and optimization of the poling process is in progress [2].
A longer-term perspective is to harness the SHG device towards twin photons generation thus paving the way for quantum applications.



Artistic view of a LN nanowaveguide cavity for efficient second harmonic generation

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30 Thin Film $LiNbO_3$Surface Preparation using SC-1

Lithium niobate ($LiNbO_3$) is a material of considerable interest in optical and nanophotonics due to its remarkable nonlinear optical properties and high electro-optic coefficient, making it ideal for integrated photonic devices, modulators, and sensors [1]. However, fabricating such devices presents significant challenges. This study investigates the fabrication challenges encountered in the production submicron surface gratings, which use $LiNbO_3$ thin films as waveguides and PECVD-deposited silicon nitride (Si_3N_4) as the grating material. A key focus is on improving the adhesion between $LiNbO_3$ and Si_3N_4, a crucial factor for stable grating fabrication. Specifically, we explore the role of SC-1 (Standard Clean 1) treatment [2] in preparing $LiNbO_3$ surfaces by effectively removing organic contaminants and redeposited by products during plasma etching of the grating.

The etching dynamics of $LiNbO_3$ of ring SC-1 treatment were studied, revealing an initially high etchingrate due to the rapid removal of contaminants and surface damage. This rate subsequently stabilizes into a linear regime, indicative of stead y-state etching. Controlled etching with SC-1 not only improves surface smoothness but also significantly enhances the adhesion strength between $LiNbO_3$ and Si_3N_4, preventing the peeling of Si_3N_4 grating patterns observed initially. The adoption of SC-1 treatment ensures robust adhesion and high-quality deposition, both essential for the performance and reliability of integrated photonic devices.

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31 Thin rib waveguides design and fabrication on LNOI

Lithium niobate (LN) is a key material for integrated photonics, not least because of its second-order nonlinear properties, which are fundamental for modulators and frequency converters operating in the material transparency range (0.4µm - 5µm). LN waveguides feature low propagation losses, making them an ideal platform for integrated photonic devices used in classical and quantum information applications [1, 2]. The advent of thin-film LN technology marks a significant step forward, meeting the growing demand for bandwidth in telecommunications and enabling non-linear processing of low-power quantum signals. Recently, high-performance optical components based on lithium niobate-on-insulator (LNOI) films have demonstrated exceptional capabilities, including record-efficient frequency converters and ultra-wideband low-voltage modulators [3, 4]. We present here our preliminary work on the fabrication of thin (300 nm thick) LNOI rib-waveguides using Ar plasma etching. Argon plasma etching tests were conducted on an inductively coupled plasma reactive ion etching (ICP-RIE) system to identify optimal etching rates for waveguide fabrication. Waveguide designs were developed using finite element method (FEM) simulations, enabling the identification of rib waveguide dimensions (widths and thicknesses) suitable for achieving single-mode propagation with reduced losses. Furthermore, an algorithm integrating modal analysis and surface roughness scattering models based on [5] was developed to estimate losses in our LNOI rib waveguides.

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LES COMPOSANTS POUR LES TÉLÉ-COMMUNICATIONS

Projet T-REX-6G

IEMN | LTM | CEA-Leti | XLIM | LAAS

Offrir aux utilisateurs mobiles un débit de données sécurisé, longue distance et haut débit est l'un des défis du XXIe siècle. Plus de 1400 To de données sont échangées dans le monde chaque minute ! Toutefois, le débit des connexions sans fil reste le goulot d'étranglement des échanges de données et il devient urgent d'augmenter les vitesses de transmission sans fil et ce sur une distance de l'ordre du km.
Le projet T-REX-6G constitue une proposition en rupture pour adresser ce défi à fort volume, en créant une chaine de fabrication intégrée de transistors III-V InP sur plaques de silicium 200mm ou 300mm de diamètre. L'ensemble du procédé technologique sera réalisé en environnement silicium. **L'objectif principal est la fourniture de transistors bipolaires à double hétérojonction InP intégré sur silicium, présentant un fonctionnement à haute fréquence jusqu'à 1THz, et permettant d'obtenir un émetteur à 300GHz de très forte puissance.**

Projet ORÖR

FOTON | C2N | INPHYNI | CEA-Leti | IES

L'imagerie THz connaît un essor important en lien avec le développement des technologies de composants intégrés semi-conducteurs et photoniques. Les applications sont nombreuses et touchent à des domaines stratégiques pour l'industrie nationale.
COMPTERA vise le développement de composants avancés pour les futurs systèmes d'imagerie multispectrale en gamme THz (0,3-30 THz) qui feront appel à des technologies très variées à la frontière de l'électronique et de l'optoélectronique, en particulier des détecteurs à haute sensibilité adaptés à chaque gamme de longueurs d'onde (notamment micro-bolomètres, détecteurs à effet de champ, photodétecteurs unipolaires à multi-puits quantiques). Une partie de ces capteurs ultra-sensibles sera ensuite intégrée à des systèmes d'imagerie adaptés à la démonstration de leurs performances.

T-REX-6G

32

Technological Development of DHBT Compatible with Si-Fab

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In a more connected world, fast and reliable communication is essential. With more data being used due to smartphones and connected devices, the sixth generation of wireless communications (6G) expected to be commercialized by 2030, will offer new solutions for faster connectivity, providing the necessary power amplification at high frequencies.
To address this challenge, this work proposes an innovative approach: integrating III-V transistors InP DHBT onto silicon substrate to combine the advantages of both technologies, with gold-free metal contacts and copper bonding on silicon wafers to ensure a full compatibility with industry standards offering better performance for high frequency and high-power applications.
In this context, we have developed Si-Fab ohmic contacts for N and P-type InGaAs based on refractory metals Tungsten (W) and Molybdenum (Mo). The best result for the N contact is 7.27×10^{-8} Ω·cm² with Mo contact, which is consistent with the value presented in the literature (5×10^{-8} Ω·cm²) for the lift-off technique associated with an ex-situ treatment. However, for the P contact, we obtain a value of 9.39×10^{-7} Ω·cm² showing that further optimization is required.
In addition, an innovative heatsink bonding based on a Si-Fab copper layer was validated with the use of copper. This latter is a material of choice thanks to its high thermal conductivity. Also, we have developed a method for InP substrate removal (grown in Collector-up configuration) using mechanical thinning down to 10 µm, followed by HCl etching.
This goal of this activity will lead to improved power performance at high-frequency for 6G-compatible CMOS integration.

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T-REX-6G

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94 GHz Power Characterization of DHBT Au-Au bonded on Si

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InP HBT technology is a good candidate for the future 6G networks that will require very high bandwidth. They have already demonstrated high-frequency operation with f_{max} exceeding 1 THz. However, this performance comes at the cost of aggressive scaling which increases thermal resistance (Rth) due to device narrowing and leads to a self-heating limiting overall performance. Transferring InP DHBTs to high-thermal-conductivity substrates has shown a drastic reduction of Rth by 65% on Si-HR and 75% on SiC thanks to their superior heat dissipation properties. While reducing Rth has shown to improve f_t and f_{max} by ~25%, its effect on output power remains little unexplored. The DHBT active layers were bonded onto a high-resistivity silicon substrate using Au-Au thermocompression followed by a conventional triple mesa process using dry and wet etching mesa definition. We present CW large-signal load-pull measurements at 94 GHz of a transferred InP/GaAsSb DHBT fabricated on a high-resistivity silicon substrate. The characterized devices feature an emitter area of 0.44 × 3.9 µm² and were biased for maximum output power. The device exhibited a power density exceeding 11 mW/µm² across various bias conditions. Its peak performance reached a saturated output power of 13.4 dBm, corresponding to a power density of 12.9 mW/µm² (5.68 W/mm), with a power-added efficiency of 23.7%. These results highlight the benefits of improved thermal dissipation in overcoming self-heating effects to achieve high output power. To our knowledge, this represents the highest reported power density for single InP DHBTs with 24% improvement compared to the previous state of the art.

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T-REX-6G

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34 Development of performant CMOS-compatible ohmic contacts for THz InP-HBT on Silicon technology

The growing demand for higher data rates in telecommunications drives 6G/sub-millimeter Wave (sub-mmW) development, targeting ~300GHz frequencies. While SiGe, GaAs, and GaN power amplifiers face efficiency limits above 200GHz, InP Heterojunction Bipolar Transistors (HBTs) are the top performers in this range [1]. However, their fabrication on small III-V substrates (100-150mm) restricts integration with antennas and digital devices, posing challenges for high-performance front-end modules. A CMOS-compatible THz HBT technology is needed for large-scale production on 300mm wafers, enabling advanced integration methods like hybrid bonding. Achieving THz frequencies requires ohmic contacts with specific resistivities around 10^{-8} Ω·cm², particularly for emitter and base contacts, as their quality directly impacts HBT frequency performance [2].

Test structures with contact dimensions ranging from 5x5µm to 0.35x0.35µm were fabricated on integrated InGaAs/InP stacks using a 200mm silicon-manufacturing platform. The contacted InGaAs layer is either 20nm thick (heavily N-doped) or 28nm thick (heavily P-doped), corresponding to the nominal emitter/collector and base contact thicknesses for the targeted THz HBT application. Contact spacing distance varies between 1.5 to 43µm. Resistivity parameters ρc and Rsh were evaluated using TLM measurements, as well as through the development of a novel numerical extraction methodology enabling more accurate resistivity assessment for such scaled contacts, with dimensions suitable for THz HBTs. Contact resistivity values as low as 5.10^{-8} and 5.10^{-7} Ω.cm² – respectively for contacts realized on N^+ and P^+-InGaAs layers – were demonstrated to be achievable using fully CMOS-compatible metallization and integration processes. Such values are encouraging for a future performant InP-HBT on Si technology.

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T-REX-6G

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35 Technological Development of DHBT on InPoSi

As we push the limits of high-speed communications and advanced photonics, the materials we rely on need to evolve. Indium Phosphide on Silicon (InPoSi) is emerging as a game-changer, combining the high-speed, low-loss properties of Indium Phosphide (InP) with the scalability and affordability of silicon. This breakthrough is paving the way for faster data transmission, next-generation 5G/6G networks, and ultra-efficient photonic circuits. The Heterojunction Bipolar Transistor (HBTs) is a powerful type of transistor that thrives at high frequencies. Unlike traditional silicon transistors, InP-based HBTs switch faster, generate less noise, and operate more efficiently, making them ideal for radio-frequency (RF) applications, millimeter-wave (mmWave) communication, and advanced radar systems. By integrating InP HBTs on a silicon platform, we obtain cutting-edge performance with the scalability of silicon manufacturing. At IEMN, the first InP/InGaAs DHBT test on InPoSi has been successfully fabricated, showing accurate DC characteristics. The fabrication of the submicron device is now in its final phase, with the process nearing completion. Additionally, both static and dynamic characterizations will be performed to assess the device's full performance.

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T-REX-6G

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LTM and IEMN HBT on InP Growth Development

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The performance of Heterojunction Bipolar Transistors (HBTs) depends largely on the quality and design of their epitaxial structure, making it a key focus in device fabrication. As these transistors continue to push the limits of high-frequency communication, low-power electronics, and ultra-fast computing, fine-tuning their epitaxial layers is essential to improve speed, efficiency, and reliability. The way these layers are structured directly impacts critical properties like carrier mobility, signal gain, breakdown voltage, and thermal management. For Indium Phosphide (InP)/Indium Gallium Arsenide (InGaAs) HBTs, precise engineering of the base, emitter, and collector layers is crucial to achieving fast switching speeds, minimal noise, and efficient power consumption, all vital for cutting-edge technologies like 5G/6G networks, radar systems, and optical communication. As part of a collaborative effort, IEMN and LTM worked together to optimize the emitter/base junction leading to the successful design of the first single heterojunction bipolar transistor (STBH) at IEMN, growth at LTM, and fabrication at IEMN. The fabricated 100x100μm² test transistor showed excellent performance, with a current gain β=Ic/Ib of 530, confirming its efficiency in common-emitter output characteristics Ic(Vce). This milestone marks a first for the Grenoble cluster, as it represents LTM's first TBH epitaxy. Taking this progress further, a submicronic 0.35x5 μm² device was fabricated, demonstrating an impressive F_T/F_{MAX} of 270/110 GHz.

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OROR

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Emetteurs OPTO-THz structurés et cohérents par photomélange à base de technologies III-V

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Les sources THz basées sur la photonique sont attractives, car elles offrent des solutions à température ambiante, reposant sur des technologies photoniques matures, tout en permettant une haute cohérence et une accordabilité large bande et une grande largeur de bande de modulation, adaptées à des applications spécifiques en THz, telles que les communications à haut débit ou la spectroscopie [1, 2]. Dans ce travail, nous présentons une source laser à base de technologie des semi-conducteurs en GaAs pour les applications THz. Nous avons développé un laser continu bi-fréquence (et un laser à verrouillage de modes passif) pompé optiquement et émettant par la surface à cavité verticale externe (VECSEL) [3, 4]. Le battement de différents modes transverses génère un rayonnement THz cohérent en utilisant des antennes photoconductrices (PCA) comme photomélangeur. Pour cela, il est nécessaire de sélectionner uniquement deux modes transverses dont la différence de fréquences se situe dans le régime THz. Nous présenterons des caractérisations optiques, spectrales et radiofréquence des deux sources laser – bi-fréquence et à deux peignes de fréquences - ainsi qu'une émission THz utilisant une PCA avec des électrodes plasmoniques, pompée optiquement à 1064 nm.

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38 Synchronized opto-mechanical oscillators for reference frequency generation and distribution

Integrated optomechanical devices strongly localize, within the same microscale cavity volume, an optical and a mechanical mode thus enhancing their mutual interaction. With a weak, on resonance optical field, the thermal motion of the mechanical mode can be read. By increasing power, the radiation pressure pumps energy into the mechanical oscillation arriving at a point in which the pump overcomes the mechanical losses. Under these specific conditions, the mechanical mode starts lasing. This regime of self-sustained oscillations is characterized by a very high and narrow peak in the RF spectrum at the mechanical mode frequency. Our cavities are one-dimensional GaP photonic crystal nanobeams suspended on top of a silicon waveguide. For our structures, a power of few hundreds μW around λ=1550 nm allows to achieve self-sustained oscillations close to 3.3GHz. Furthermore, this architecture allows us to locate several cavities on top of the same waveguide such that, when their optical and mechanical resonances are close enough, they can couple through light showing synchronization regimes. Thanks to a controlled thermal-optical shift of the first fundamental optical modes, we control their overlap. Simultaneously, the mechanical modes evidence synchronization for a given pump wavelength range. With an additional low power probe laser, we independently read the oscillations of both, verifying the synchronized regime. Finally, we demonstrate an all-optical integrated platform to generate and distribute an in-phase reference frequency at two different wavelengths. These two low power signals show stability performances, in terms of phase noise, comparable to ones of the high-power pump signal.

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39 Preliminary characterization of an Integrated Ring Resonator for the Development of Optoelectronic Oscillators

The generation of microwave signals with high spectral purity is essential for many applications, such as radar and telecommunications [1]. Optoelectronic oscillators (OEOs) have been studied over the years as convenient devices for the optical generation of microwaves signals [2]. A basic OEO typically use a long optical fiber (several kilometers). However, today's systems require these devices to be integrated into photonics chips of a few square centimeters.
In this context, integrated ring resonators, used as photonic filters, have emerged as excellent alternatives to optical fibers. The frequency and spectral purity of the microwave signal generated by an OEO are directly linked to the Free Spectral Range (FSR) and quality factor (Q-factor) of the ring resonator [3]. Therefore, we must first of all accurately characterize these resonators.
In this work, we characterized an integrated Silicon Nitride (SiN) ring resonator fabricated at CEA-LETI (Fig. 1). We slowly swept the laser frequency across the resonance of the ring resonator, and spectrally analyzed the transmitted light using the Component Analyzer feature of a Brillouin Optical Spectrum Analyzer (BOSA Aragon Photonics). This yielded a FSR of 9 GHz and a Full Width at Half Maximum (FWHM) of 100 MHz (Fig. 2). This corresponds to a Q-factor of 2×106. A further characterization of the dynamical response is in progress, involving rapid laser wavelength sweeps over a duration shorter than the resonator lifetime [4]. This allows a complete characterization of the parameters of the resonator.

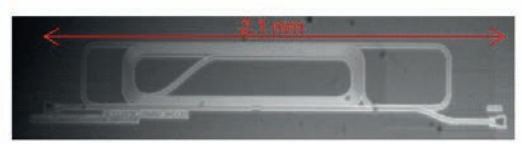
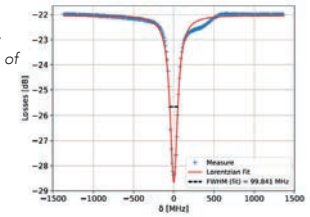


Fig.1: Picture of the ring resonator under study

Fig.2: Transmission as a function of the frequency detuning for a resonance of the ring resonator



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L'ÉLECTRONIQUE POUR LE CALCUL

Projet EMCOM

SPINTEC | LTM | CEA-Leti | Lab. A. Fert | IJL | LIRMM

La performance énergétique des processeurs conventionnels étant désormais dominée par le coût du transfert de l'information entre les différentes strates de stockage et les unités de calcul, des innovations de rupture sont nécessaires en termes d'architecture, mais aussi de composants électroniques permettant de rapprocher voire fusionner les fonctions de calcul et de mémoire.
Si les mémoires magnétiques semblent avantageusement positionnées pour répondre aux critères d'endurance et de vitesse associés à ces nouveaux paradigmes, les caractéristiques de la génération actuellement en production demeurent insuffisantes. **Au cœur de ce projet ciblé, des dispositifs innovants issus de la recherche fondamentale permettant notamment de découpler lecture et programmation, viseront à adresser les verrous qui persistent, tout en évoluant vers des solutions compatibles avec les standards de fabrication industrielle.**

Projet BEP

FEMTO-ST | C2N | INPHYNI | IM2NP | IRAMIS | Lab. A. Fert

Le projet BEP vise à réduire considérablement la consommation énergétique de l'électronique pour le calcul. Il s'inspire pour cela du cerveau qui connecte de façon dense, tridimensionnelle et reconfigurable ses unités de calcul, les neurones. Notre stratégie consiste à combiner l'électricité et la lumière, qui permet des connexions 3D ultra-denses pour imiter l'architecture du cerveau. Nous développerons par ailleurs des technologies mémoires imitant les synapses, permettant à nos circuits d'apprendre, comme le fait le cerveau. Enfin, nous réaliserons des nano-neurones interconnectés capables de calculs extrêmement complexes avec peu de composants. Toutes les différentes briques seront intégrées dans des technologies CMOS pour réaliser des calculs bio-inspirés. Elles donneront les fondations pour une plateforme cognitive intégrant les différentes stratégies du cerveau pour calculer et économiser de l'énergie.

Projet FERROFUTURES

IMS | INL | IM2NP | CEA-Leti | CEA-List | CEA-Iramis

L'Internet des objets (IoT) requiert le déploiement d'une intelligence artificielle (IA) de proximité, l'IAe, qui devra répondre aux exigences en termes de très faible consommation, de faible latence, de traitement temps réel, et de confidentialité. La technologie ferroélectrique possède un potentiel inégalé notamment en termes de consommation d'énergie permettant d'accéder à des fonctionnalités non-volatiles à un coût très bas et une efficacité surpassant celle des technologies concurrentes.
Sur la base des travaux pionniers sur la fabrication de mémoires ferroélectriques HZO ($HfZrO_2$) bien plus respectueuses de l'environnement que ses prédécesseurs à base de plomb PZT ($PbZrTiO_3$), **le projet FerroFutures propose une approche de co-optimisation entre la technologie, le circuit et le système qui sera mise en œuvre selon deux axes :**

- **l'optimisation d'un composant ferroélectrique (FeMFET) à basse tension, avec une endurance supérieure à 10^{12} cycles, une lecture non destructive, et son intégration en circuits innovants pour le calcul embarqué à base de microcontrôleurs ;**
- **la conception de circuits et d'architectures en rupture pour la réalisation d'un système de calcul (vectoriel) de type data logger haut débit (≥100Mo/s) sur la plateforme du CEA MAD200 dont le démonstrateur donnera lieu à une puce de test.**

EMCOM

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40 Stochastic magnetic component networks for low power cognitive computing

Traditional von Neumann architectures struggle with performance and energy efficiency when tackling complex computational challenges, such as NP-hard combinatorial optimization problems. Recent proposals have emerged with the aim of building specific hardware accelerators inspired by the Ising model. The expected benefits stem from their amenability to executing local search algorithms with Simulated Annealing (SA), while processing the data locally and minimizing explicit update instructions. Ising machines can be described as recurrent neural networks with binary stochastic activations.
In this work, we combine stochastic Magnetic Tunnel Junctions (sMTJ) as neurons interconnected by an OxRAM coupling array for the weights. We present the characterisation of MTJ devices integrated in the Back-End-Of-Line of a CMOS chip, as well as the resolution of NP-hard optimisation problems, including small-sized graph partitioning problems (Max-Cut and Graph Coloring). Those problem instances were solved experimentally by combining two hybrid technologies (CMOS+memristors, CMOS+MTJ).

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41 Three terminal devices for improved efficiency

Spin-orbit torques (SOT)-based magnetic tunnel junctions (MTJ) are promising candidates for embedded non-volatile memory applications due to their ultra-fast dynamics (sub-ns), high endurance (1012−16), and low power operation (sub-pJ) [1]. In these structures, a charge current flows through a non-magnetic heavy metal (HM) and is converted to a spin current via the Spin Hall effect (SHE) and Rashba-Edelstein effect (REE) [2]. In turn, the spin current applies a torque on the adjacent magnetic free layer (FL) that stores information, as shown in Fig.1(a).
A critical challenge for SOT-MRAM technology is reducing the write current (I_{write}), which depends on the charge-to-spin current conversion efficiency (ξ). While β-tungsten remains the state-of-the-art conversion layer [1], recent studies suggest leveraging orbital physics to enhance ξ further [3]. Materials like Cr, Ti, Al, and Ru show potential, but experimental demonstrations of improved SOT-MTJ switching with these materials are limited [4].
This study explores Ru as an orbital source in three-terminal (3-T) structures, employing heavy metals to convert the orbital current into spin current. These heavy metals act both as spin source (via SHE), and as orbital-to-spin conversion layer (for the strong spin orbit coupling). Initial experiments involve simplified Hall-bar stacks to investigate the impact of various materials and layer thicknesses on ξ, Fig.1(b). In a second step, promising systems are optimized and integrated into full SOT-MTJ devices with diameters as small as 50 nm, enabling electrical characterization and comparison of material systems, Fig.1(c). Preliminary results indicate improved conductivity for the Ru samples, though ξ improvements remain inconclusive. This work seeks to clarify the role of orbital-to-spin conversion in advancing SOT-MRAM technologies for memory and neuromorphic applications.

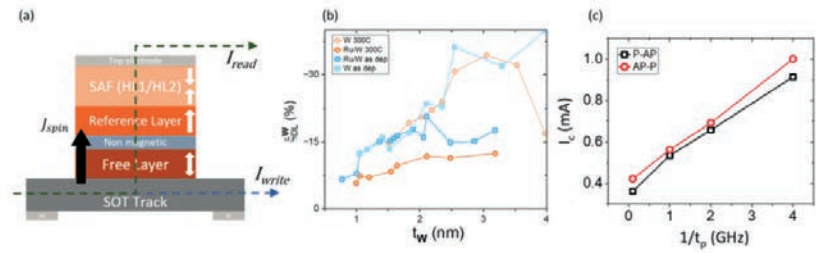

Fig.1 (a) Schematic representation of a SOT-MTJ. (b) Annealing effect over ξ. (c) Ic-tp dependence for a W sample

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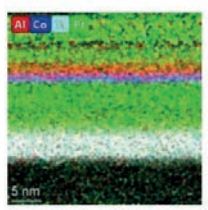
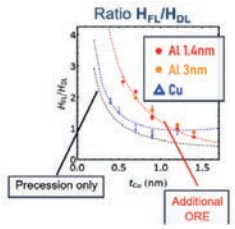
42

From spin to orbital control of the magnetization in ultrathin cobalt

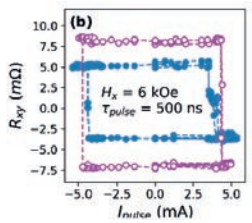
Searching for more efficient electrical control of magnetization dynamics through Spin-Orbit Torques (SOT) is at the heart of today's spintronics research. Indeed, it is crucial for the emergence of SOT-MRAM as both fast and energy efficient non-volatile memory technology. The most established proposals for SOT generation rely on heavy metals (Pt, W or Ta) grown in contact with the ferromagnetic layer to control the magnetization. However, it has been shown that growing Al on top of an ultrathin Co ferromagnetic layer induces large SOT through an orbital Rashba effect [1, 2]. This poster will display the experiment leading to these results and exhibit new investigations on the physical origin of SOT. Varying the thicknesses of the different layers in this system, we show to what extent CoAl interface affects spin-dependent transport and enhances the torques. We also display how adding Spin-Orbit Coupling (SOC) in this interface through Pt dusting cancels out the effect. This shows how the strong Rashba effect is sensitive on the interface quality and that adding SOC doesn't straightforwardly increases the torques. Finally, we show how SOT from CoAl is relevant to current driven magnetization switching experiments in nanopillar based devices.



EDX elemental map of the multialyers



Comparison of the SOT amplitudes



Current induced magnetization switching

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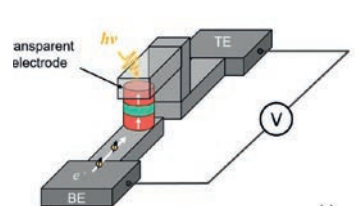
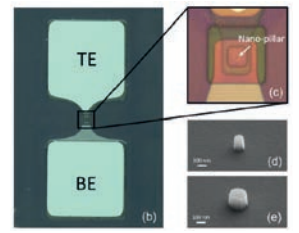
43

Towards ultrafast deterministic switching in magnetic memory by laser excitationg

Recent advances in ultra-fast switching in magnetic memory have been made possible by fs and ps pulse laser excitation of magnetic tunnel junctions (MTJs) integrated with Tb/Co multilayers [1, 2]. The underlying mechanism behind the magnetization reversal relies on the precessional motion of the ferromagnetic layer initiated by the demagnetization induced by the laser pulse [3, 4]. Fabricated MTJ devices with tunnel magnetoresistance (TMR) up to 74% showed consistent all-optical switching (AOS) magnetization reversal under 50-fs laser pulses [5]. However, the dependence of the magnetization reversal on the precessional motion of the magnetic moment implies that the magnetic state cannot be deterministically defined from the point of view of memory storage. Our current work addresses a possible deterministic switching in AOS-MTJs devices by combining the ultrafast localized heating from the laser pulse with the spin-polarized current (Fig. 1a). Macrospin simulations have successfully indicated the possibility for the spin-polarized current to impact the optically induced magnetic switching of the ferromagnetic system. During the precessional motion of the free layer, the spin-polarized current exerts a torque on the magnetization, driving it to eventually relax in the desired magnetic state. These findings serve as an essential theoretical basis for conducting this experiment on manufactured nanopillar devices (Fig. 1b). Simultaneously, in the stack of AOS-MTJ structure, the oxidation conditions of the Mg layer were optimized to achieve both high anisotropy and thermal stability with a thin tunnel barrier. These improvements reduce the resistance area of the AOS-MTJs stack for compatibility with spin-transfer torque effects to assist the magnetic switching during the precessional motion, as predicted by the simulation results.

Figure 1: Schematic illustration of AOS-MTJ devices under the effect of laser excitation and spin-polarized current (a); Microscope image of the final patterned AOS-MTJs device (b); The close view of a fabricated window with an underlying nano-pillar (c); SEM images of nano-pillar devices with different diameters: 100 nm (d), and 200 nm (e).





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44 Study and optimization of ferroelectric $Pb(Zr,Ti)O_3$ thin film for emerging spintronic and electronic devices

The increasing power consumption of information and communication systems is driving the need for a new type of low-power electronics. Ferroelectric materials, with their remarkable properties, are ideal for low-power, high-speed memory and logic applications. Two innovative designs have emerged: Ferroelectric Tunnel Junction (FTJ), which utilizes polarization switching to modulate electrical resistance,
and the Ferroelectric Spin Orbit (FESO) device, which used the ferroelectric control over spin-charge interconversion in a 2D electron gas. $Pb(Zr,Ti)O_3$ (PZT) is a strong candidate for these designs due to its exceptional remanent polarization, endurance, and low coercive field. This work focuses on optimizing PZT thin film growth using Pulsed Laser Deposition (PLD). Structural properties, analyzed via x-ray diffraction and scanning probe microscopy, confirm the high quality of the grown layers. Various polarization states were observed using Piezo Force Microscopy (PFM), showing that growth conditions influence film chemistry. With a view to fabricate FTJs, we grew ultrathin PZT films, down to 20 Å, in which ferroelectricity was confirmed using PFM. After defining FTJs with a top electrode of Co, electrical measurements were conducted with an RF pulse generator and a picoamperemetre to study the tunnel electroresistance. In parallel, in order to explore the potential of PZT for FESO, a 2DEG was induced on the PZT surface by depositing an aluminum layer, and the interface structure characterized using XPS and STEM. This presentation will discuss the growth, structural, and functional attributes of these samples, providing insights into the challenges of creating a 2DEG and FTJs based on PZT.

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45 Design of Hybrid Nanodevices/CMOS Systems for Optimization and Artificial Intelligence Applications

Nanodevices offer multiple opportunities to make energy-intensive tasks performed on computers more efficient, specifically optimization and artificial intelligence applications. For instance, superparamagnetic tunnel junctions are new spintronic components, leveraging both the electric and magnetic properties of electrons, which can naturally toggle between two binary states due to thermal noise in a completely random manner. Such devices can generate random bits with very low energy consumption, and they can serve as foundational units for 'Ising machines,' an emerging computation model inspired by the structure of magnetic materials. This model is especially suitable for certain optimization and machine-learning problems. However, an electronic system based on superparamagnetic tunnel junctions cannot operate solely using these passive components. It also requires active elements. This research aims to design the CMOS circuits to be paired with superparamagnetic tunnel junctions to create low-power consuming Ising machines. The project demands the design of various circuit types: analog circuits for junction control, and mixed analog/digital circuits to bridge the gap between the junction domain, adapted memory circuits, and the purely digital CMOS functions responsible for communication among the system's fundamental units. These circuits, which will also utilize superparamagnetic tunnel junctions and other types of nanodevices, will be assessed based on process, voltage, and temperature variabilities, fabricated by our partners within the PEPR Electronic program, and tested extensively.

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46 Trade-offs in Neural Network Compression: Quantized and Binary Models for Keyword Spotting

Enabling smart and independent IoT devices often requires to run complex Machine Learning (ML) workloads at the edge [1]. Such systems usually operate with memories in the order of tens of kilobytes and low processing power. To fit within these constraints, model designers typically rely on lowprecision integer representation of operations down to 1-bit, i.e., Binary Neural Networks (BNN) [2]. We investigate the tradeoffs available to model designers between memory footprint and accuracy and the challenges to overcome for effective use of BNN. We show that designing BNN architectures is not a straightforward process [4]. To overcome this, we propose a methodology based on design guidelines and Neural Architecture Search (NAS) [3] to adapt traditional model architectures into BNN variants. As a case study, we apply this methodology to a ResNet-based model for a keyword spotting (KWS) application. Our results demonstrate that, contrary to 8-bit quantization, direct binarization significantly impacts accuracy. However, careful architecture redesign and hyperparameter tuning helps bringing BNNs performances on par with their quantized counterparts.

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47 Design of an arithmetic logic unit (ALU) using ferroelectric spin orbit (FESO) devices

While transistor size and voltage scaling have allowed CMOS technology to offer a continuous increase in computing efficiency, it is now close to its technological limit. Indeed, the progressive increase of leakage attributed to the Boltzmann Tyranny has led to the end of Dennard's law. In this context, new spintronics based devices have recently been proposed as beyond CMOS candidates such as the MESO (MagnetoElectric Spin Orbit) device of Intel which exhibits memory and logic properties and has the potential to operate at the aJ scale [1]. These performances are possible thanks to a low power ferroelectric-based writing of the memory and a magnetoelectric coupling enabling a spin charge interconversion (SCI) based readout of the memory. This allows the device to work as a memory and produce an output charge current enabling logic. More recently, the FESO (FerroElectric Spin Orbit) device has been proposed by the Spintec laboratory with the same low power computing properties as the MESO device [2]. However, it is a simpler concept that gets rid of the magnetoelectric element thanks to a direct control of the SCI by the ferroelectric state. In this work, we present a compact model for the FESO device, simulated in the Cadence virtuoso environment. Using this model, we demonstrate the suitability of the FESO device for sequential and combinational logic. The FESO based basic elements for an ALU (majority gate, multiplexer, full adder, multiplier) are conceptualized and simulated to build a 4-bit FESO based ALU. The benefits in terms of area and energy consumption of the approach are evaluated.

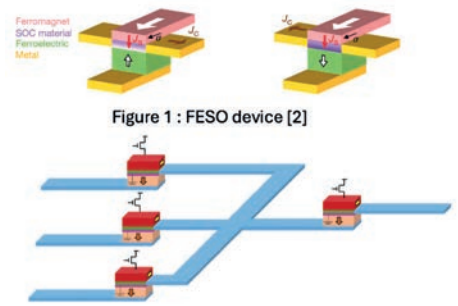
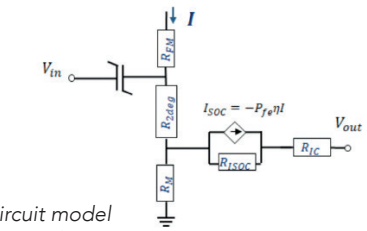


Figure 1 : FESO device [2]

Example of FESO based logic gate



Equivalent circuit model for FESO device

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48 Ultrafast dynamics, from the modelisation to first applications

The knowledge and fundamentals of demagnetisation dynamics is of significant importance for understanding many spintronics applications (All Optical Switching, THz emission). In this frame, we have developped a complex model to accurately describe the optical demagnetisation of ferromagnetic materials in multilayer systems subject to short laser pulse [1, 2, 4]. This model has been applied to a simple yet interesting system constituted by a Co(2nm)/Pt(4nm) bilayer, which is widely studied and known as a spintronic THz emitter. Our model using local heating, diffusive transport, thermal gradients and spin-charge conversion phenomena has obtained promising results when applied to this system. Our simulations show a remarkable behavior comparable to the ones found in the recent literature [3, 4]. Regarding THz emission, we were able to obtain THz emission spectra $E_{THz}(\omega)$ comparable to the experimental ones [5].

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49 Implementing Equilibrium Propagation on CMOS

Ferroelectric nanoelectronic devices are fully compatible with conventional electronics CMOS technology and feature very controlled dynamics that resemble behaviors of synapses and neurons in the brain. The study aims to implement a novel deep learning approach, partially inspired by how the brain works, Equilibrium Propagation, which can take advantage of ferroelectric technologies particularly well. Equilibrium Propagation is a physics-inspired artificial intelligence approach. The physics of ferroelectricity can be embedded within the core principles of this approach, with the potential to lead to highly energy-efficient AI.

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50 Hafnium Oxide Ferroelectric Films: from fundamental understanding to optimized low power device Integration

Neuromorphic systems are artificial neural systems inspired by the biological human brain, whose connections can be mimicked by artificial synapses between memory devices, forming neural networks (NN) for deep learning. Training a NN demands plasticity, which requires the possibility to analyze a large number of values stored in memory and allow changes in synaptic strength. Inference, in turn, demands long-term stability. Currently, no non-volatile, low-power memory technology offers both characteristics simultaneously.
In the pursuit of a memory solution for simultaneous on-chip learning and inference, a hybrid FeRAM/OxRAM synapse circuit is proposed. Hafnium oxide (HfO_2)-based ferroelectric memories (FeRAM) are used for learning, exploiting their high endurance, ultra-fast, low-power (10-50 fJ/bit), and non-volatile character. However, the destructive read operation of FeRAMs makes them unsuitable for inference. This is why HfO_2-based resistive memories (OxRAM) are used for inference, as they offer long-term stability and non-destructive reading. A successful development and implementation of an OxRAM/FeRAM synapse on a single CMOS substrate requires a comprehensive characterization of the physico-chemical properties of the HfO_2 layer to understand their impact on the performance of the device [1]. Manifest interest has been given to oxygen vacancies (VO) point defects, which appear to have a preeminent influence on the endurance. Here we illustrate the capabilities of hard x-ray photoelectron spectroscopy (HAXPES) for VO quantification and profiling in HfO_2. By inserting an ultra-thin, metallic, oxygen scavenging layer it may be possible to engineer the required vacancy concentration and hence optimize the ferroelectric/resistive character.

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51 Forward-Forward Learning Exploiting Low-Voltage Reset of RRAM

Analog RRAM is highly efficient for on-chip inference, providing important energy savings [1]. However, on-chip learning poses greater challenges due to complex data movement and the need for higher device accuracy [2]. This capability is essential for edge applications such as health monitoring and predictive maintenance. In 2022, Geoffrey Hinton introduced the «Forward-Forward» algorithm to address these challenges, predicting that it would be robust against the imperfections of memristors [3]. Despite this promising proposal, significant adaptations of the initial algorithm are required to confirm Hinton's intuition.
In this work, we present the first version of the Forward-Forward algorithm specifically adapted for high energy efficiency learning with resistive memory. We validate our approach using extensive measured statistical data from a dedicated prototype in-memory computing platform equipped with 8k RRAM cells employing a TiN/HfOx/Ti/TiN stack. We first introduce three adaptations to the Forward-Forward algorithm for compatibility with RRAM, and optimize the low-voltage RESET regime of RRAM to attain a noise level acceptable for the Forward-Forward algorithm. Then, by co-optimizing device programming conditions and the algorithm, we achieve high-accuracy heartbeat classification based on real ECG measurements, in a hybrid hardware/software simulation using actual RRAM measured data rather than model simulations. Finally, we highlight that the reliance on low-voltage RESET offers significant advantages in terms of energy efficiency, device retention, and endurance, crucial for applications requiring reliable and sustainable on-chip learning.

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52 On Chip Customized Learning on Resistive Memory Technology for Secure Edge AI

Learning-capable edge AI systems are crucial for secure and personalized applications in user-specific environments, such as medical diagnosis or predictive maintenance. By enabling model customization directly on inference hardware, on-chip learning eliminates the need for cloud-based data and model sharing, ensuring privacy and security. Despite its potential, this approach is challenged by the energy- and time-intensive nature of training. ReRAM, with its promise of improved energy efficiency through in-memory computing, offers a compelling solution. This work presents the first experimental validation of few-shot on-chip training on an in-memory computing resistive memory (ReRAM) platform using the Model-Agnostic Meta-Learning (MAML) algorithm[1]. To reduce training iterations and associated ReRAM conductance updates, the neural network is pre-trained off-chip. Through co-optimization of device programming conditions and the algorithm, we achieve high accuracy on the Omniglot dataset after just five training iterations (*i.e.*, ReRAM programming operations) while also significantly improve device retention.

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BEP

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53 A novel optical communication concept for electronic chips for next generation neural network accelerators

The integration of photonics with advanced computing architectures presents transformative opportunities for the future of information processing [1]. This research, explores the synergistic combination of three-dimensional (3D) photonic integration with CMOS electronic integrated circuits (ICs), incorporating memristive programming to enable neuromorphic computing capabilities [2]. The electronic IC, features silicon photodiodes, enabling efficient light detection. A central innovation lies in the use of III-V lasers for electro-optic conversion, facilitating high-speed data transmission, while 3D polymer waveguides are employed to establish long-range optical interconnects. This photonic platform aims to overcome the energy and latency limitations of conventional electronic communication in neural network computing frameworks, as well as the exponential interconnect growth respect to area of 2D circuits compared to linear growth for 3D circuits [3]. By leveraging the unique properties of light for data transmission and computation, the integration of photonics enables massive parallelism, low-energy operation, and high-bandwidth interconnects-key enablers for advanced neuromorphic systems. Furthermore, in this work the 3D photonic circuits are designed to be all-optically reconfigurable. The fully integrated chip will be characterized to validate its functionality, marking a significant step toward hybrid photonic-electronic computing platforms.

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54

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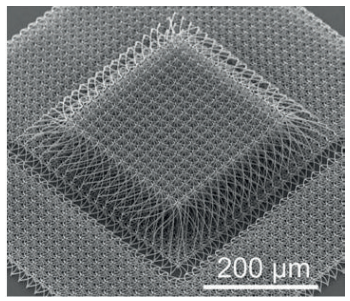
Development and Application of 3D Integrated Photonics for Neuromorphic Computing

Since the advent of computing, there has always been demand for faster and more efficient devices. As conventional computer architectures approach their physical limits and AI becomes increasingly prominent, addressing this demand has become not only more challenging but also more preeminent [1], [2]. One promising research direction involves novel integrated, brain-inspired, low-power hybrid opto-electronic computing systems to overcome the limitations of traditional computing paradigms [3].
A significant bottleneck using conventional electronic hardware for AI tasks arises from the intensive computation required for large-scale matrix operations. Our work addresses this challenge by exploring optical methods for performing these operations. Leveraging state-of-the-art 3D printing techniques, it is possible to fabricate low-loss, micrometre-scale, CMOS compatible 3D polymer waveguides [4]. Arranging these waveguides on a 3D grid (see figure [5]) and using the intensities of spatially multiplex light as the input vector, we show how to designing a 3D photonic circuit such that it performs the optical matrix multiplication on the inputs' intensities. Moreover, we show that finding the correct arrangements of waveguides such that it corresponds to a desired matrix can be formulated as an optimisation problem that can be solved via a simulated annealing-inspired algorithm. We envisage, the photonic circuits may offer an effective passive means of implementing efficient in-memory computing ideally suited for inference tasks thus, paving the way for integrated opto-electronic neuromorphic computing.



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Antiferroelectricity in $PbZrO_3$ thin films under epitaxial tensile strain

Antiferroelectrics possess a compensated antiparallel arrangement of electric dipoles, resulting in a zero net polarization[1]. Applying an electric field across an antiferroelectric triggers a volatile transition to a ferroelectric phase, giving rise to double hysteresis of polarization vs. electric field. This property makes antiferroelectrics very attractive for applications such as high-energy density storage, and electronic devices based on antiferroelectric tunnel junctions are envisioned as artificial neurons[2]. The antiferroelectric nature of lead zirconate, $PbZrO_3$, the historical[1] and most studied antiferroelectric material, has recently been challenged[3]. Progress in the synthesis of high-quality materials and characterization using scanning transmission electron microscopy has revealed the complex nature of the polar textures in $PbZrO_3$, with the apparition of ferrielectric (i.e. uncompensated antipolar state) phases even in single crystals[4], and complex ferrielectric or ferroelectric phase transitions in ultrathin films[5,6]. While first principles calculations suggested that tensile strain could stabilize antiferroelectricity down to nanometre scale7, $PbZrO_3$ epitaxial thin films are usually grown on commercial oxide substrates with large lattice mismatch, which leads to fast strain relaxation. Here we demonstrate pure antiferroelectric behaviour in $PbZrO_3$ ultrathin films epitaxially grown under tensile strain on artificial substrates of $LaLuO_3$. Sharp double hysteresis of polarization as a function of electric field in capacitors based on such $PbZrO_3$ films do not show any remanent polarization. On the other hand, local atomic maps of polar displacements reveal the characteristic antipolar pattern down to nine nanometre film thickness. These results unlock the path to functional antiferroelectric devices based on coherently strained $PbZrO_3$ ultrathin films.

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FERROFUTURES

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56 Compact modelling of ferroelectric memory devices for compute-in-place applications

In the rapidly evolving field of nanoelectronics, ferroelectric components, with distinct characteristics such as nonlinearity and hysteresis, hold the potential to be used in advanced memory devices. By integrating ferroelectric capacitors on top of MOSFETs to form Ferroelectric Memory FETs (FeMFET), we can leverage their unique properties to create memory architectures with enhanced performance. Additionally, this integration significantly enhances retention capabilities, paving the way for more efficient and reliable memory systems. This integration holds great promise for advancements in Compute-In-Place applications, offering a pathway to more advanced and high-performing computing systems. The current research focuses on developing a compact, current-based model for ferroelectric memory devices, accurately characterizing their complex behavior. The proposed model will be validated and optimized through extensive simulations against experimental data, showcasing its potential for performance enhancement and energy efficiency of next-generation computing systems. By incorporating this compact model written in Verilog-A into tools like CADENCE, designers can optimize memory architectures for improved computational efficiency. In its current state, our current-based model captures the essential dynamics of ferroelectric capacitance, providing detailed insights into its impact on overall device performance. This study also explores the scalability of ferroelectric memory devices, highlighting their potential for integration into large-scale computing systems. This research not only demonstrates the feasibility of integrating ferroelectric components into advanced memory architectures but also underscores the impact of such integration on enhancing computational efficiency and reliability of ferroelectric devices.

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57 Design of hardware accelerator for in memory Computing based on Ferroelectric Devices

When considering a Von-Neumann architecture-based hardware to compute data intensive algorithms, it is now clearly admitted that the main contribution to energy consumption comes from data movement between CPU and memory [1]. This limitation is known as the memory wall [2]. Enhancing memory with computation functionality, in order to keep data stationary, is a vast and dynamic research domain, that could solve the memory wall issue. Moreover, to keep the information in the memory even when the power is off, emerging nonvolatile memories are a great asset. In this context, emerging CMOS-compatible HfO2 based FeRAM technology could bring real breakthroughs to computing in memory due to its exceptional features (low-voltage, high endurance and energy- efficiency etc...). However, since this technology is still in its infancy, investigation at circuit level through dedicated test-chips is necessary to assess all necessary features for in-memory computing.

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LES ACTIONS CONCERTÉES TRANSVERSES

Projet ADICT

CRHEA | IEMN | Lab. A. Fert | SPINTEC | CEA-Leti

L'objectif de cette action concertée transverse est d'adresser les verrous qui bloquent jusqu'à présent l'intégration des matériaux bidimensionnels (Matériaux 2D) dans la filière électronique. Ces matériaux 2D n'ont pas été adoptés jusqu'à présent par une filière industrielle malgré les performances remarquables au niveau des composants individuels. **Nous proposons de montrer qu'il est possible d'obtenir des matériaux 2D monocristallins sur de grandes surfaces (taille du substrat), de pouvoir former des empilements d'hétérostructures complexes** soit par croissance in situ, soit par report par collage avec contrôle de l'angle d'empilement et d'intégrer ces matériaux sur une plateforme silicium. En s'appuyant sur le développement avancé des matériaux et des technologies de report, nous ferons la démonstration de composants à base de matériaux 2D qui pourront répondre aux enjeux de certains des projets ciblés du PEPR Électronique.

Projet PAC

RENATECH | CEA-Leti

La R&D en laboratoire conduit à des PoC trop rarement déployées en milieu réel. En effet le packaging est le chaînon manquant. Les laboratoires développent des expertises et investissent, avec trop peu d'interactions avec toute la communauté. Enfin, le Packaging est souvent perçu plus comme une problématique d'ingénierie que scientifique.
Pour lever ces obstacles **l'AC-PAC :**

- **coordonnera les moyens/compétences pour optimiser l'usage des ressources, formaliser l'expression collective des besoins. Cette coordination perdurera au-delà du PEPR.**
- **coordonnera des développements spécifiques, et lèvera des verrous technologiques du PEPR Électronique, ou d'autres PEPRs.**
- **anticipera des besoins émergents.**
- **associera les moyens académiques (CNRS, Universités) et préindustriels (CEA-Leti).**

Projet CHOOSE

CEA-Leti | SPINTEC | INL

CHOOSE vise à développer une solution de co-optimisation technologie, circuit intégré et système. Il s'agit d'une approche originale intégrant toute la chaîne de valeur de la conception depuis les modèles des technologies jusqu'au benchmarking applicatif, en prenant en compte les outils de conception/synthèse et de simulation de circuits et d'architectures, les données des processus de fabrication, les aspects logiciels, compilateurs. Les études porteront sur les architectures d'accélérateurs de calcul utilisant des paradigmes avancés tels que le calcul approximé, vectoriel ou encore stochastique. CHOOSE permettra de projeter les développements technologiques du nano-composant unitaire sur la conception et les performances de circuits et d'architectures complexes pour les applications avancées.

ADICT

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58 Growth of MoS_2 Using Molecular Beam Epitaxy

Since the synthesis of graphene in 2004 [1], interest in two-dimensional (2D) materials has significantly increased, particularly focusing on transition metal dichalcogenides (TMDs) such as molybdenum disulfide (MoS_2). These materials offer exceptional electronic, mechanical, and optical properties at the atomic scale, and their bandgap is tunable depending on the number of layers [2], making them ideal for advanced electronic, and optoelectronic devices. However, synthesizing high-quality 2D materials on an industrial scale remains a challenge. Although Chemical Vapor Deposition (CVD) and Pulsed Laser Deposition (PLD) offer more scalable alternatives, they encounter issues related to thickness uniformity and purity control. In this context, Molecular Beam Epitaxy (MBE) has emerged as a leading technique for growing TMDs (such as MoS_2), thanks to its precise control over deposition parameters and the ability to monitor growth in situ using techniques such as Reflection High-Energy Electron Diffraction (RHEED).

Our study demonstrates a growth of MoS_2 layers on GaN/sapphire substrates using Molecular Beam Epitaxy (MBE). Morphological characterization via Atomic Force Microscopy (AFM) revealed the formation of triangular MoS_2 domains on the GaN surface. Raman spectroscopy analysis of the E^1_{2g} and A_{1g} modes showed distinct peak separations, confirming the formation of monolayer and bilayer MoS_2 on the GaN substrate. High-Resolution Scanning Transmission Electron Microscopy (HR-STEM) was employed to investigate the interface between MoS_2 and GaN.

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59 TMD Engineering of 2D-Magnetic Tunnel Junctions – From Barriers to Electrodes

Spintronics has revolutionized data storage, notably through the development of highly sensitive hard-drive read-heads based on Giant Magnetoresistance (GMR), and later Tunnel Magnetoresistance (TMR) technologies. These are at the core of Magnetic Tunnel Junctions (MTJs), nowadays composing the latest generation of ultra-fast and low power Magnetic Random Access Memories (MRAMs) and fueling post-CMOS unconventional electronics strategies (including spin logics, stochastic, neuromorphic and quantum computing). In this direction 2D materials [1] have unleashed a multitude of previously unexploited possibilities for spintronic devices. As such, graphene has already demonstrated impressive performance, achieving record spin polarization of up to -98% in a MTJ [2]. But more recently, a new class of materials, 2D ferromagnets, have emerged as particularly promising for spintronics, as they could pave the way to gate-controllable 2D magnetic tunnel junction (2D-MTJ) spin valve devices. However, a 2D ferromagnet efficiently working at room temperature remains a clear challenge. In this work, we focus on the development of room temperature 2D ferromagnets and their integration as electrode into 2D-MTJs. Specifically, we have engineered 2D ferromagnets based on Fe_4GeTe_2. To achieve this, we have recently developed novel in-situ processes based on large-scale pulsed laser deposition (PLD) techniques to allow the growth and heterostacking of different 2D materials [3]. We will discuss how to reach one step further with the large-scale integration of these materials into tailored 2D heterostructures.

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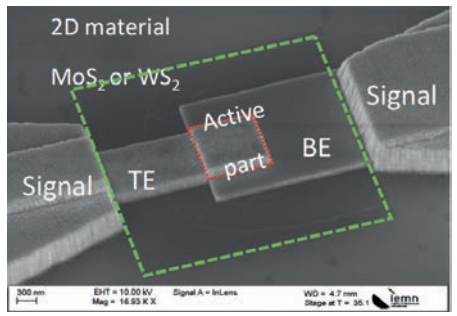
60 Fabrication of RF switches based on MoS_2 and WS_2

In the framework of the ADICT project, the partner IEMN-CARBON aims to produce components based on 2D materials [1-3], for targeted PEPR projects. The aim is to extract their electrical properties and propose applications for high-frequency analogue electronics. The first components to be explored are RF switches based on 2D materials.
Our work has led us to develop technological processes that are compatible with those of our partners (CEA Leti). The material used is MoS_2 by ALD (Atomic Layer Deposition) growth, requiring a wet or dry transfer step. The growth and the fabrication process are managed on a 200 mm silicon substrate.
This approach will be compatible with materials obtained by MBE (Molecular Beam Epitaxy) growth.
A second approach has been developed with our partners at LAF, where 2D materials (WS_2) are obtained by PLD (Pulse Laser Deposition) growth, requiring no transfer step, given the lower thermal budget.
The performance of the devices obtained is in line with the simulations carried out at IEMN. The performances obtained are already state-of-the-art for this type of component.

Active zone of a RF switch



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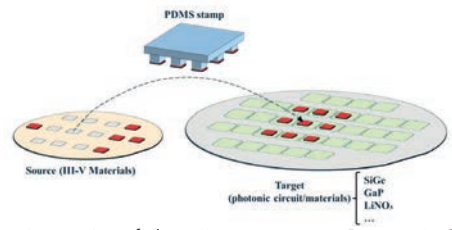
61 Exploring Micro-Transfer Printing for Heterogeneous Integration for Emerging Applications

Micro-transfer printing (µTP) is a promising technique that enables the heterogeneous integration of diverse materials onto highly versatile platforms with high precision and efficiency. Traditional integration methods often face challenges such as material incompatibility, thermal mismatches, and fabrication complexity, which hinder the realization of hybrid devices with optimal performance. µTP addresses these challenges by offering a scalable, low-temperature, and flexible approach to transfer and integrate a release layer onto different substrates [1-2]. In our work, we first explored µTP to successfully integrate an interband cascade laser (ICL) onto silicon (Si) and silicon-germanium (SiGe) platforms, overcoming the limitations of conventional integration techniques. During the µTP process, certain selected factors influencing transfer alignment accuracy have been studied, including the effects of different applied forces and temperatures during transfer, as well as the thickness and softness of the polydimethylsiloxane (PDMS) stamps used. Our investigations revealed critical insights into optimizing transfer accuracy and yield, which are crucial for ensuring reliable transfer and device performance. Characterization of our integrated devices demonstrated efficient carrier injection and reliable light emission, validating the feasibility of this approach for photonic device applications [3]. Beyond this initial success, we aim to expand the scope of µTP to explore the integration of other advanced materials, including gallium phosphide (GaP), lithium niobate ($LiNO_3$) and emerging two-dimensional (2D) materials. These advancements are expected to enable a wide range of applications, such as communication, sensing and quantum devices. This work highlights the promising future of µTP in heterogeneous integration and next-generation photonics.

Fig. 1. Schematic diagram illustrating the integration of III-V materials onto a target for obtaining optimal performance.



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62 Innovative Applications of µAM in High-Frequency Component Design: From 3D Structures to Coplanar Line Repair

This communication introduces the first attempts to repair coplanar lines using three distinct methods: conventional interconnections, interconnections printed with the electrodeposition micro-AM machine [2], and the complete recovery of missing metallic material at the break points using the same technology. The µAM process, based on localized electrochemical deposition, enables to print precise metallic 3D structures with micrometric resolution. It allows the direct deposition of conductive materials with properties similar to bulk metals, ensuring material continuity in damaged areas.

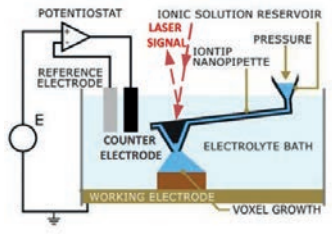

Fig. 1.

Fig. 2a

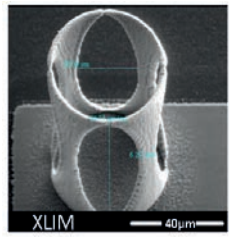

Fig. 2b

Fig. 1. Schematic of the µAM process: The setup includes the ionic solution reservoir, nanopipette tip, electrolyte bath, and the working, reference, and counter electrodes. The laser signal tracks the nanopipette tip deflection to monitor voxel growth in real time. Adapted from [1].
Fig. 2.a micro bridges, b. 3D micro-structure, all printed with Copper using the µAM technology.

The study evaluates the feasibility of these approaches to restore both electrical and mechanical functionality of broken coplanar lines. The electrodeposition micro-AM machine is specifically utilized to reconstruct missing metallic sections layer by layer, achieving accurate alignment and structural integrity [3], [4]. By integrating these repair methods with photolithography processes, hybrid solutions are explored for maintaining performance in high-frequency components.
This communication focuses on detailing the methodologies employed in these repair attempts, providing a comparative framework for these innovative approaches. These efforts serve as a basis for future evaluations aimed at optimizing repair strategies and enhancing their suitability for very high frequency applications up to 600GHz.

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CHOOSE

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63 Méthodologies émergentes pour la co-optimisation système-circuit-technologie pour le calcul proche-mémoire

Common memory technologies used in advanced computing devices are constrained by three main factors: power, performance and area. With the growing demand for artificial intelligence applications, such systems based on the von Neumann principle face a major bottleneck, related to the huge amount of data movement and the associated energy and latency costs.
To address this challenge, memory-centric compute architectures have been proposed, in which some computational tasks are processed within, or close to, memory units.
Indeed, the two main groups within these architectures are: «Near-Memory computing» and «In-Memory computing». The former reduces the distance between the computing and memory units, and the latter integrates processing directly in the memory unit, both approaches reducing the global data movement.
These new paradigms however open up a vast design space, whether in terms of technology (emerging non-volatile technologies at the device level) or architecture. Therefore, many tools have emerged for design space exploration. They are either memory-level simulator, such as NVSim [1], or architectural-level simulators.
We propose a multi-level exploration environment that establishes a link between memory technology and architecture via a hierarchical descriptive memory model and a simulator based on SYSTEMC-TLM [2]. A Python-based cockpit is used for iterative architectural and technological refinement to identify optimal solutions. The goal is to evaluate the potential of emerging technologies developed at an early stage, linking Design-Technology and System-Technology Co-Optimization (DTCO/STCO) approaches, and to provide the best possible guidance for future technological choices in relation to the architectures and circuits for data-intensive applications.

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64 Dramatically Improving Energy Efficiency in AI through In-Memory Computing Integration in Programmable RISC-V Systems

Artificial Intelligence (AI) has revolutionized many fields, yet its implementation is associated with substantial energy consumption. This energy constraint is a significant barrier, particularly for embedded applications and resource-limited devices. Recent advancements in in-memory computing, using innovative components like memristors and MRAM, have shown remarkable potential to drastically reduce this energy consumption. However, for flexible use in almost all applications, these in-memory computing circuits need to be integrated into programmable systems. Integrating in-memory computing into programmable systems poses major challenges, including the potential loss of energy benefits due to data movement and potential bottlenecks. This issue is especially pronounced during the AI model training phase, which requires high programmability and flexibility.
This thesis aims to develop hybrid architectures combining in-memory computing and RISC-V programmable systems, with an intense focus on optimizing this interface and developing rigorous methods for evaluating energy consumption.

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CHOOSE

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65 MRAM-Based Crossbar Design for In-Memory Computing

Machine Learning (ML), particularly through Convolutional Neural Networks (CNNs), is widely used in edge applications like image recognition, sound classification, and fraud detection. However, CNNs are energy-intensive [1] due to frequent data transfers between memory and processing units in traditional CPU-centric systems. In-memory computing (IMC) mitigates this issue by processing data near storage, significantly enhancing energy efficiency and throughput.
However, IMC systems face energy challenges from analog-to-digital converters (ADCs) [2]. While advanced ADCs and emerging alternatives like Time-to-Digital Converters (TDC) [3] [4] show promise, their efficiency and applicability depend on eNVM technology and workload demands.
Our goal is to develop an ADC scheme tailored for MRAM-based IMC architectures, leveraging both the advantages offered by MRAM, such as its high resistance, speed, and energy-efficiency and its limits such as its binary nature and stochastisity.
We address these through a first design of a 64×64 crossbar design incorporating current-controlled oscillator (CCO) readout circuit for improved precision, dynamic range, and process variation resilience, while simplifying post-fabrication calibration.
On the software side, we optimize model architecture, weight precision, and sizing. The initial design demonstrates near-perfect accuracy on the MNIST dataset, achieving 30 TOPS/W energy efficiency and robustness against fabrication variations. Ongoing efforts aim to further enhance efficiency and evaluate performance on complex ML tasks like keyword spotting. Integration into a RISC-V-based SoC is also planned for holistic co-design across abstraction layers.

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66 A Reliable 22nm Ferroelectric-based Non-Volatile SRAM Optimized for Critical Embedded Systems

Ferroelectric-based non-volatile SRAMs (nvSRAM) are one of the most promising solution that combines the fastest volatile memory (SRAM) and one of the most energy efficient emerging non-volatile memory (HZO-based ferroelectric capacitance, FeCAPs). An nvSRAM bitcell consists of an SRAM bitcell within which non-volatile BEOL ferroelectric capacitors (FeCAPs) have been integrated. This hybrid bitcell can then perform four different operations: (1) reading from SRAM (READ op.), (2) writing to SRAM (WRITE op.), (3) copying data from SRAM to FeCAPs (STORE op.) and (4) transferring data from FeCAPs to SRAM (RECALL op.). The resulting memory is thereby fast, energy efficient and non-volatile while being able toperform massive parallel STORE and RECALL ops. In this work, we use 6T4C nvSRAM bitcells [Fig. 1] incombination with a previously developed fast-erase mechanism [1] to (i) ensure fully functional RECALLeven with SRAM ops. between STORE and RECALL, and (ii) counter cold-boot attacks while keeping datain the non-volatile part [Fig. 2].
In a previous work [2], we demonstrated in simulations that reliable nvSRAM operations are achievable thanks to the fast-erase circuit and an optimized FeCAP sizing in a 130nm CMOS technology node. To go further, we now project these results on a 22nm CMOS technology node. All results come from SPICE simulations based on Monte-Carlo analyzes and a VerilogA model calibrated with silicon measurements on FeCAPs devices.

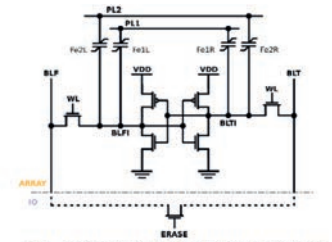

Fig 1. 6T4C nvSRAM bitcell with Fast-Erase

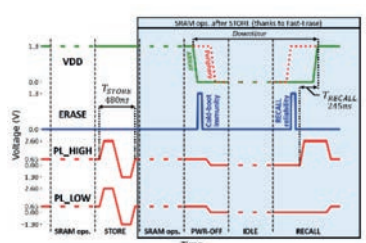

Fig 2. Operations chronogram

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Acknowledgement: ANR-22-PEEL-0013

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